A CMOS Baseband Receiver for Wireless Broadband Communications

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***Abstract*— This paper presents an UWB baseband receiver including VGAs, LPFs, FGAs and IO buffers, fully integrated in 130nm CMOS process. The voltage gain range by two VGAs and a FGA for each I/Q path is from -5 to +65dB providing a dynamic range of 70dB. For a more stable operation against variations in process, voltage and temperature (PVT), the cut-off frequencies of our receiver can vary from 183 to 548MHz by changing 3dB bandwidths of a LPF. The LPF consists of three biquads having different bandwidths and Q factors. The core area of our baseband receiver is about 600um X 1000um. The receiver without an IO buffer draws only 13.4mA from a 1.5V supply for each I/Q branch.**

***Keywords*— CMOS, UWB, LPF, VGA, baseband receiver**

I. INTRODUCTION

The required bandwidth of short-range wireless communications increases rapidly to meet the demand for high-speed data services, such as the wireless universal serial bus (WUSB), the wireless IEEE 1394 and HD-quality video transmissions between a TV and a set-top box. The communication systems operating at millimeter-wave frequencies can support such high data rate transmissions. However, they consume high power due to both high channel attenuations and low gain efficiencies of a transistor over the transmission frequency band. Also, it is difficult to ensure reproducibility of the communication systems because circuits over the extremely high operating frequency range are easy to be unstable. It is preferable, therefore, to use communications below 10GHz for accommodating the short-range high speed data services with low power and stable systems for commercialization.

Among several wireless transmission systems operating lower than 10 GHz, the ultra-wideband system (UWB) is regarded as the most practical one, since it eliminates the need for additional frequency allocations and dissipates very low power due to its low transmit power regulation, improving the battery time of its products. Thus, much effort has been directed toward implementing UWB communication systems by many companies, universities and research institutes across the world [1]-[4].

In this effort, we present a baseband receiver including VGAs, LPFs, FGAs and IO buffers for an UWB radio frequency transceiver as shown in Fig. 1. We mainly discuss

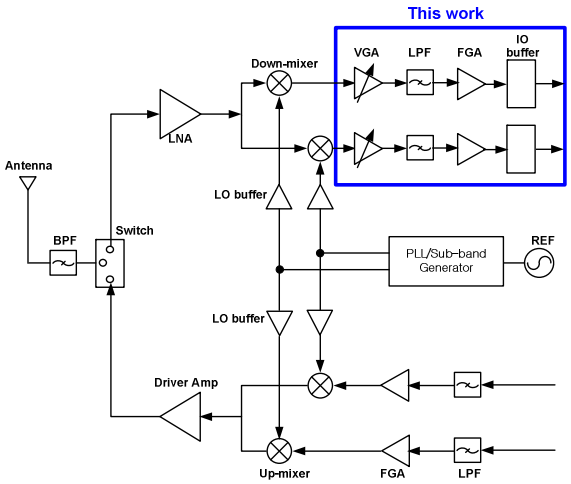


Figure 1. The designed baseband receiver in our UWB RF transceiver

operation principles, circuit implementations and simulated performances of a LPF, a VGA and the entire baseband receiver, not a FGA or an IO buffer in this paper. Our UWB baseband receiver is fully integrated in 130nm CMOS process for a low power and low cost implementation through one chip solution with MODEM.

II. LOW PASS FILTER

A low pass filter plays an important role in channel selection and suppression of interferers in modern wireless communication systems. In particular, a low pass filter in a direct-conversion receiver as shown in Fig. 1 must have high attenuation performance at stop-bands to meet selectivity specifications because there is no intermediate stage providing additional suppressions at the stop frequency bands. With the requirement of a low pass filter for our UWB RF transceiver shown in Fig. 4 [5], a low pass filter in the UWB receiver could provide not only high rejection ratio at adjacent channels but also a wide bandwidth operation capability.

Among several kinds of wideband filter architectures such as Gm-C, switched capacitor and active RC filters, we have chosen the Thomas biquad structure based on active RC filters. This is because, with the architecture, high cut-off frequencies

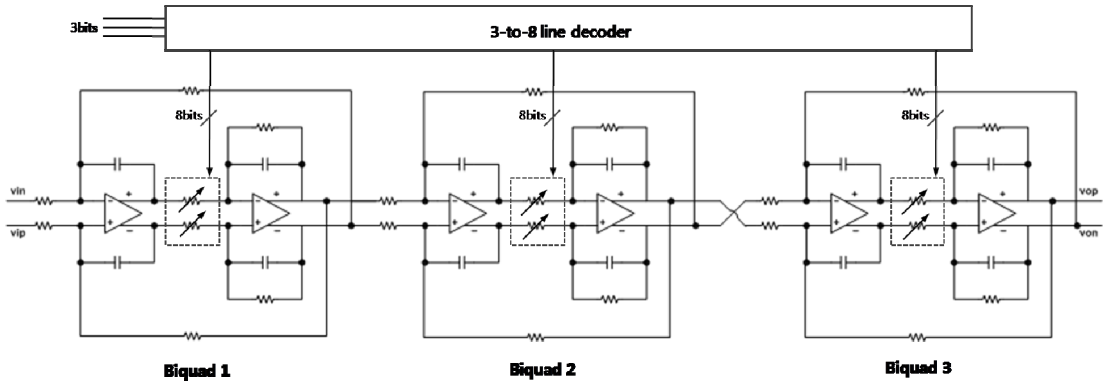


Figure 2. The structure of the six-order Thomas biquad LPF

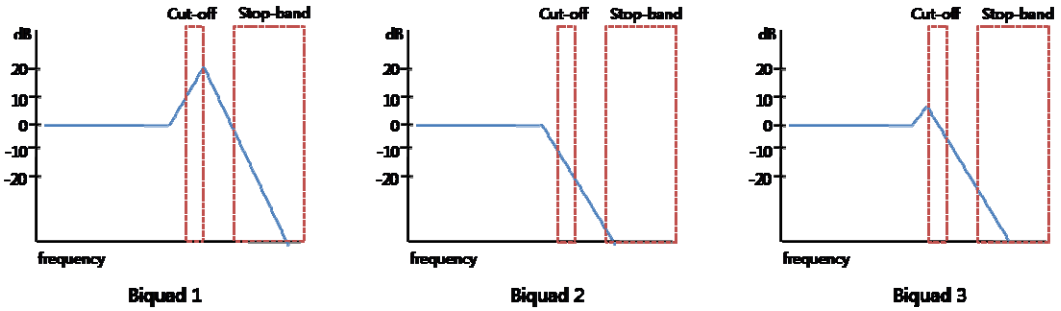


Figure 3. Three different frequency reponses of the three biquads

up to 264MHz with a good rejection performance and better linearity characteristics can be achieved [5]-[7].

Fig. 2 shows the overall structure of our designed low pass filter. It consists of three biquads having three different bandwidths and Q factors to obtain a wide bandwidth while achieving a good stop-band attenuation characteristic as shown in Fig. 3. The three biquads are connected in cascade so that the overall frequency response is determined by a combination of the frequency responses of the three biquads. To obtain a high rejection ratio at stop band, the all biquads show attenuations at the stop frequency ranges of around 285 and 520MHz. However, to make the 3dB bandwidth of the entire filter higher than 264MHz, the first biquad has a high positive peaking characteristic at the cut-off frequency while the other two biquads show attenuations at the frequency band to compensate the peaking.

For a more stable operation against process, temperature and voltage variations, bandwidth tuning circuits were also implemented. 3 bit digital signals are decoded to 8 bits to control resistances for each biquad by turning on/off switches. A wide tuning range of 3dB bandwidth from 183 to 548MHz has been achieved with the digital tuning circuit.

III. Variable Gain Amplifier

Another key building block in an UWB baseband receiver is a variable gain amplifier to provide automatic gain control (AGC) to the following stage so that it can properly process

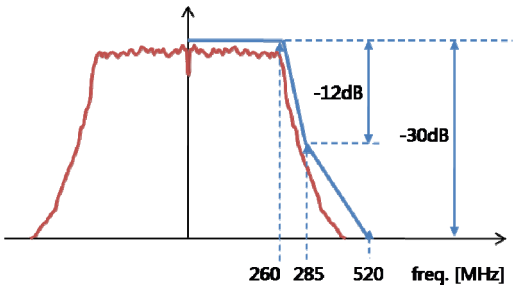


Figure 4. The requirement of a LPF for an UWB communication

received signals and recover original user data from the signals.

Fig. 5 shows the circuit of the proposed VGA which consists of mainly two blocks. One block as a gain stage is a modified version of the Gilbert cell with a cascode structure, for high dynamic range, high gain, and broad bandwidth. The other block is an active load for wideband operation by using inductive peaking with a source follower and a capacitor for each output branch. There is also a bias current steering circuit to obtain a higher dynamic range. It controls bias currents of the VGA input stages by changing gate voltages of M7 and M8 as a gain control voltage of Vcont varies.

In the input stages (M1~6) in Fig. 5, M1~M4 operate mostly in triode regions while all the other transistors operate in saturation regions. This is because trans-conductance of a MOSFET in triode mode can be controlled by its drain-source voltage of Vds directly related to gain control voltage Vcont, so

that the voltage gains are changed as shown in equation 1. Here, we don't consider M3 and M4 at this time for simplicity.

$$G_m = \frac{g_{m1}}{1 + g_{ds1}/g_{m5}} \quad (1)$$

where, $g_{m1} = \mu_N C_{OX}\left(\frac{W}{L}\right)V_{DS1}$, $g_{ds1} = \mu_N C_{OX}\left(\frac{W}{L}\right)(V_{GS1} - V_{THN1})$

In the active loads (M13~16, C1 and C2), output voltage signals are fed to gates of M14 and M16, main loads of our VGA, through source follower M13 and M15 as well as C1 and C2. Since the two capacitors of C1 and C2 are connected in parallel with the gates of M14 and M16, high frequency signals are attenuated at the gates, thereby affecting less the output branch Vo(+) and Vo(-), which results in a higher voltage in output branches. Thus, we can obtain inductive peaking at our active loads. The impedance of our active load at Vo(-) is given by the following equation 2 [8].

$$Z_o = \frac{C_1}{g_{m13}g_{m14}}\left(s + \frac{g_{m13}}{C_1}\right) \quad (2)$$

As a result, the voltage gain of our VGA is described by equation 3

$$A_v = -\frac{g_{m1}}{1 + g_{ds1}/g_{m5}} \cdot \frac{C_1}{g_{m13}g_{m14}}\left(s + \frac{g_{m13}}{C_1}\right) \quad (3)$$

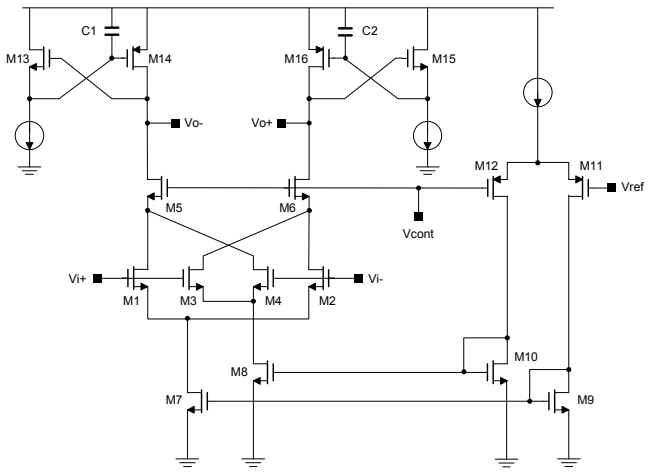


Figure 5. The structure of the VGA

IV. Baseband Receiver for UWB

The block diagram of our baseband receiver for UWB communications is shown in Fig. 6.

Each I/Q branch consists of two VGAs, a LPF including three Thomas biquads, a fixed gain amplifier (FGA) and an IO buffer. The gain of a FGA is 20dB to meet the required signal level at the output. An IO buffer is used in order to a drive low resistive load through PADs.

Fig. 7 shows designed baseband blocks in the chip photograph of our developed UWB RF transceiver (3mm X 3mm). It s core size not including PADs is 600um X 1000um.

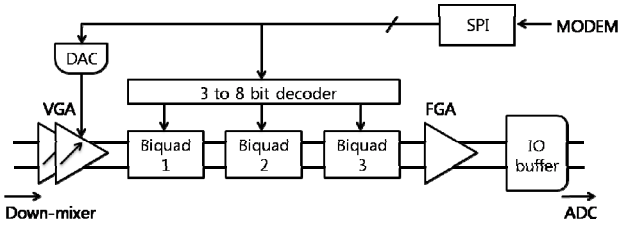


Figure 6. Block diagram of the UWB baseband receiver

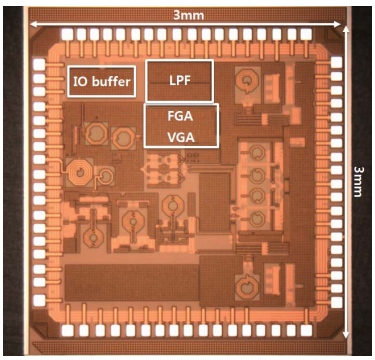


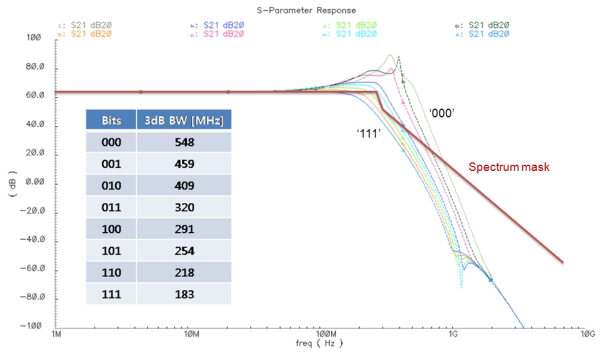
Figure 7. Chip photograph of our UWB RF transceiver

V. Post-Layout Simulation Results

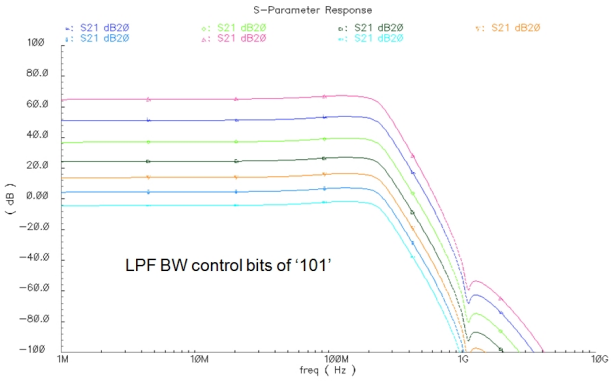
Fig. 8 shows frequency responses and variable gain characteristics of our overall baseband receiver with RC parasitic components after layout. Its 3dB bandwidth can be controlled from 183 to 548MHz through 3 bit control data, providing the tunable bandwidth range of 365MHz.

In the case of control bits of '111' or '110', stop band attenuation requirements of -12dB at 280MHz and -30dB at 520MHz are well satisfied. Even though the attenuation at 280MHz with control bits of '101' is slightly lower than the requirement, it is anticipated that the digits are more likely to be used when our baseband receiver works together with other blocks such as MODEM through bonding or package interface. Actually, the stop band performance with bits of '101' will meet the attenuation requirement at 280MHz due to bandwidth shortage effect by parasitic components of external devices.

In the case of control bits of '000', '001' or '010', however, the peak excursions are too high to be used for signal transmissions, which definitely invites and exacerbate signal quality problems, resulting in poor bit error rate (BER) performance. Thus, it seems to be difficult to choose those control digits in a real transmission system. But, if our communication system is suffered from a huge bandwidth shortage problem by parasitic components, they also will be able to be used for bandwidth compensation.



(a) Freuqncy tuning characteristics vs. BW control words



(b) Frequency responses with different voltage gains

Figure 8. Post-layout simulation results of our receiver

The voltage gain of our baseband receiver is mainly determined by two VGAs and a FGA. As shown in Fig. 8(b), the gain range is from -5 to +65dB, providing a dynamic range of 70dB with the LPF bandwidth control bits of '101'. Each VGA provides a voltage gain range of 35dB from -12.5dB to +22.5dB while the gain of the FGA is fixed at +20dB. Because of not enough gain of the cascade VGAs in our receive chain for link budget, the FGA is used for high output voltage level. The VGA gain control is performed by MODEM through SPI and DAC. For simple implementation, R-2R ladder architecture was chosen for the DAC. The performance of our whole UWB baseband receiver is summarized in Table I.

VI. CONCLUSION

We have designed and simulated an UWB baseband receiver including LPFs, VGAs, FGAs and IO buffers which is fully integrated in 130nm CMOS process. To compensate the signal quality deterioration by variations in process, voltage and temperature, 3dB bandwidth of the reciever can be controlled from 183 to 548MHz through an LPF bandwidth tuning signal in 3bits. The total gain range provided by our receiver is -5 to +65dB for a 70dB dynamic range needed for link budget. The receiver core area excluding PADs is 600um X 1000um. Without IO buffers, it draws only 13.4mA from a 1.5 supply for each I or Q branch.

Table 1. Performance Summary

Parameters	*Results*	*Etc.*
Technology	130nm CMOS	
Core area	600um x 1000um	
Supply voltage	1.5V	
Current consumption	13.4mA	for each I or Q path (Except IO buffers)
Gain range	70dB	-5 ~ +65dB
Filter architecture	6th order Thomas biquad	
Cut-off frequency	183 ~ 548MHz	controlled by 3bit digital data
Noise Figure	Typ. 12dB	Max. gain at 100MHz

ACKNOWLEDGMENT

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