A Pipelined Division for Fixed Operation Using User-defined Floating Point

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***Abstract*—A pipelined division arithmetic for fixed operation using user-defined floating point is proposed in this paper. Division operation is difficult in fixed operation, the dividend A is firstly converted into user-defined floating point, then the inverse is implemented in the invertor unit. B/A will complete with a fixed multiplication. Linear approximation theory and Newton-Raphson iteration are used in invertor unit.**

The major advanced of this arithmetic is that it easily combines with fixed operation, we can proposed user-defined floating point according to the range of dividend A and the accuracy can easily acquire. In this paper, invertor unit for A range to [0.5, 2) with 23 decimal bits is designed. It is compiled and implemented both on FPGA and Synopsys Design Compiler.

***Keywords*—division, linear approximation, Newton-Raphson iteration, FPGA, Synopsys Design Compiler**

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