Accelerating a Radio Astronomy Correlator on FPGA

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Abstract— **Radio astronomy correlator shows its significance in astronomical measurements. However, computational cost presents a barrier because of the increasing of the array size as well as the number of antennas. So the correlators which deal with signals coming from all the antennas are extremely computationally intensive process. Efficient usage of hardware should be explored in order to meet this computational challenge. This paper focus on the most computationally expensive parts in radio astronomy correlator and accelerate it using single FPGA. Results shows that the proposed hardware designs speed up the computation by at least 150 times compared with single thread CPU implementation, and at least 4 times compared with FPGA design without optimization. The throughput of our design is also higher than fully parallel CPU solution for at least 10 times, and defeats FPGA implementation without optimization in most cases.**

Keyword—**radio astronomy, FPGA, High Level Synthesis, hardware acceleration**

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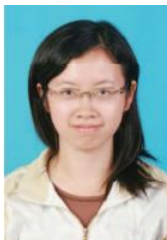
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