Data alignment for multi-channel high-speed interfaces using PRBS patterns

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***Abstract*—Multiple FPGAs are used for high-speed and large amount of data transfer and also designed to implement DSP functions. The consecutive PRBS patterns are used for bit synchronization and data alignment between high-speed multi-channel interfaces of FPGAs.**

***Keyword*—bit synchronization, data alignment, multi-channel I/O, PRBS patterns**

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