

Design and Implementation of an Optoelectronics Chipset for Automotive Wired Network

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Abstract— In this paper, an optoelectronics transmitter and receiver chipset is designed and implemented for automotive wired network using 0.5- μm CMOS technology. In fiber optic transmitter (FOT), modulation current has to be arranged in 3 to 4-mA to meet eye protection regulations in visible red wavelength (650-nm). To apply for low cost POF applications, simple and low cost FOT is proposed. FOT is designed to operate at 50-Mb/s bit rates and consumes only 6-mA DC currents including modulation current of 3.5-mA. In the receiver side, two methods of auto-threshold control technique will be introduced and compared. The designed fiber optic receiver (FOR) achieves trans-impedance gain of 145-dB Ω , 50-Mb/s operations with 45-MHz bandwidth for 4-pF photodiode parasitic capacitance. And proposed fiber optic receiver guarantees digital level output swing against the range of incident photo current from 200-nA to 25-uA and the range of operating frequency from DC to 50-Mb/s. Receiver chipset consumes only 10-mW from a 3.3-V single supply.

Keywords— Optoelectronics, Automotive wired network, fiber optic transmitter, fiber optic receiver, CMOS

I. INTRODUCTION

Recently, electronic devices have rapidly replaced a number of mechanical components in automotive vehicles. Playing a major role in controlling the whole system, the electronic devices in a luxury car cost more than 25 percent of the total manufacturing cost. Moreover, analysts in car-industry estimate that more than 80 percent of all the automotive innovations stems from electronics. Among the novel innovations, there is an automotive network which is used either to interconnect electronic equipments or to control the vehicle-body components, as shown in Figure 1. The POF is the most leading candidate for automotive wired networks.

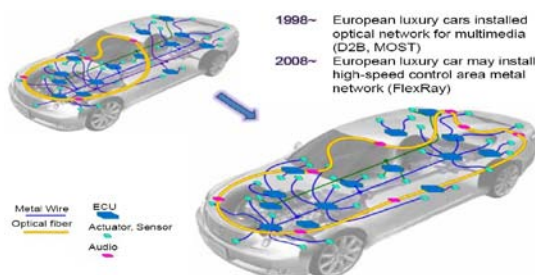


Figure 1. Automotive wired network

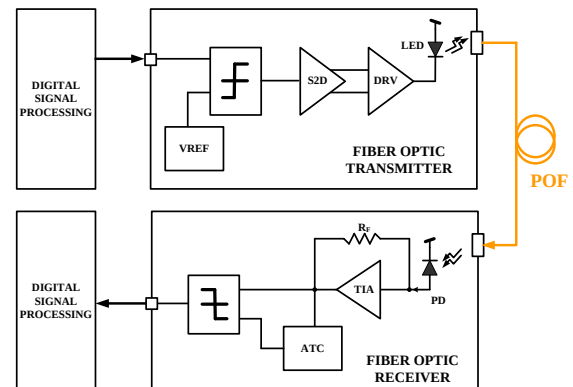


Figure 2. POF optical transceiver system

Plastic Optical Fiber (POF) is very low in cost and also permits the use of low-cost interconnection because its core size can be larger than other fibers (almost 1-mm in diameter). However, it has a loss of about 180-dB/km when operated in the low-loss window at 650-nm wavelength (visible red region). It is therefore restricted to short distance applications, such as high definition digital audio interface, automotive networks, and consumer electronics [1].

Figure 2 shows the block diagram of POF optical transceiver. In POF optical transceiver, the most important parameters are their cost and current consumption. Thus, Fiber optic transmitter (FOT) and fiber optic receiver (FOR) for POF should have simple structure, while being satisfied with system requirements such as digital I/O level, the large range of operating frequency, and the large input dynamic range. Contrary to high speed optical transceiver for glass optical fiber applications, the input and output levels of POF optical transceiver is full digital level (0V~VDD) for subsequent and previous digital signal processing block.

The proposed fiber optic transmitter and receiver in details will be introduced in Section 2 and 3, respectively. In Section 3, the measurement results will be discussed, and the conclusions will be given in Section 4.

II. FIBER OPTIC TRANSMITTER

A. Structure and Circuit Design

It is well known that the optical source devices, such as light emitting diode (LED), laser diode, and vertical cavity surface

emitting laser (VCSEL), are driven by current signal, not voltage signal. Thus we can say the optical transmitter is the current driving circuit with required bandwidth, driving current, and input dynamic range. The 650-nm FOT has to have simple structure and low power consumption to apply low cost POF applications, as shown in Figure 3. It consists of comparator, biasing block, single to differential pre driver, and main current driving circuit.

The FOT has only four I/O pads for its simplicity, that is, we have no additional pad for biasing control. Therefore, simple and reliable internal bias circuit is required. To reduce the supply dependency of bias voltage, the supply-independent (SI) bias circuit is exploited, as shown in Figure 4. It is well known that this bias circuit has supply-independent output current, if we assume the source-to-body voltage equals to zero. And we can control bias current and voltage by determining the mirroring factor (K). Conventional SI bias circuit exploits passive resistor, and its value (R_s) considerably affects the output currents [2]. To avoid process variation of poly resistor, we use the NMOS transistor (N_{M3}) as a resistor operating in triode region.

Typically, the input level of FOT is full digital level, ground to supply voltage. However, we inserted the comparator as an input stage to apply various types of input level. The comparator generates the digital level output against the wide input swing range from 0.4-V to 3.3-V. The comparator is designed using DC level-shifter and conventional differential common-source amplifier, and its reference voltage shares SI bias voltage, $V_{DD}/2$. DC level-shifter converts the dc level of input signal into half supply voltage using source follower.

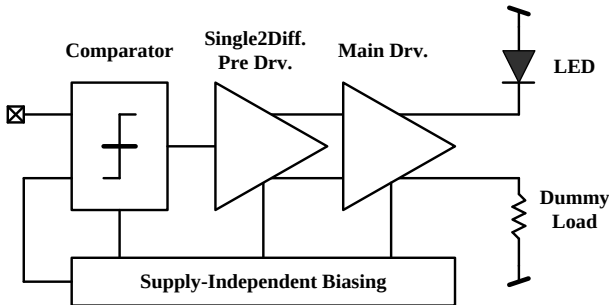


Figure 3. 650-nm fiber optic transmitter

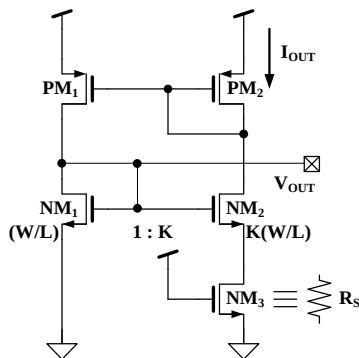


Figure 4. Supply-independent bias circuit

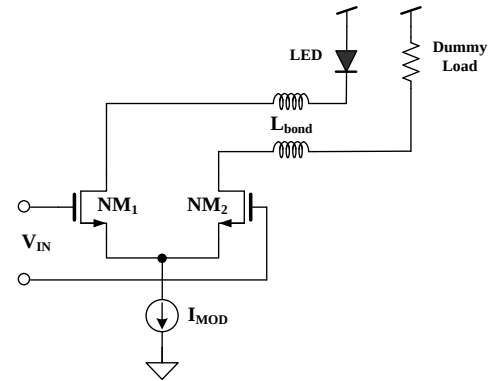


Figure 5. Main driver

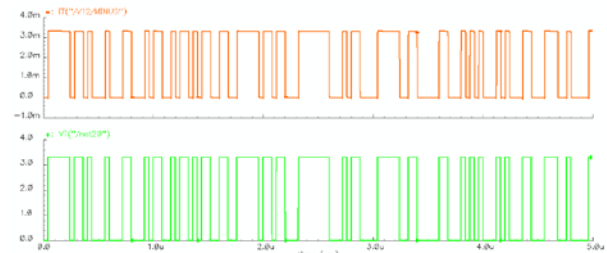


Figure 6. Transient response (@50-Mb/s PRBS31)

For stable and constant current driving capacity, the main current driver has differential structure with dummy loads. And comparative large size of switching transistors is required in main driver for sufficient current driving capacity. Therefore, the single to differential pre driver should be needed to drive these large transistors. The pre driver has the topology of conventional differential common-source amplifier with half supply voltage reference. Owing to the pre driver, the main current driver can have sufficient large switching transistor. The differential main current driver is shown in Figure 5. As mentioned above, the modulation current of FOT has to be limited to the range of 3 ~ 4-mA for eye protection against light. Therefore, the current source is designed to meet this requirement against variation of supply, process, and temperature variations. The simulation result will be introduced in next section. The 650-nm LED is operated by main current driving circuit, and the typical output optical power is -8 to -12-dBm. Another output of differential driver is connected to an on-chip resistor dummy load, 100-Ω. This value is not critical, thus, diffusion resistor is exploited as a dummy resistor.

B. Post-layout Simulation Results

Figure 6 shows the transient response for 50-Mb/s pseudo-random bit sequence (PRBS) input. The results show very short rising and falling time, under 10-psec, and 3.3-mA modulation at 3-V supply voltage. The upper and downer waveform indicates 50-Mb/s PRBS input and output driving currents, respectively. The modulation current should have limited range of 3 ~ 4mA against supply variation. Figure 7 shows the output driving current according to supply variation. From 2.6-V to

III. FIBER OPTIC RECEIVER

A. Structure and Circuit Design

The graph plots Driving Current [mA] on the y-axis (ranging from 2.50 to 5.00) against Supply Voltage [V] on the x-axis (ranging from 2.50 to 3.90). The data points show a linear relationship. Two red arrows point from the x-axis to the data curve: one at 2.6V pointing to approximately 2.55 mA, and another at 3.7V pointing to approximately 4.0 mA. Horizontal dashed red lines are drawn at 3.0 mA and 4.0 mA.

Above explained, FOR for POE applications should operate at wide frequency range from DC to 50-Mb/s. Therefore, we cannot choose the differential structure. Figure 8 shows the proposed fiber optic receiver. FOR has single-ended structure due to above reason. And FOR should have digital level output swing (3.3V) and wide input photo current range from 200-nA to 25-uA. Thus, we choose simple common-source trans-impedance amplifier, auto-threshold control stage, and comparator.

The auto-threshold control (ATC) block is the most important in this single-ended structure. The performance of ATC determines the degree of pulse-width distortion (PWD) error. In POF applications, especially high-definition digital

[illegible]

To overcome above two drawbacks, different type of ATC is proposed. The proposed ATC consists of is 6-dB attenuator and top hold circuit, shown in Figure 12. The 6-dB attenuator provides a half signal of input, and the top-hold circuit detects and maintains the maximum level of the half signal. The open-loop voltage gain of OPAMP affects the accuracy of 6-dB attenuator and top-hold circuit. Therefore, OPAMP is designed to gain-booster folded cascade structure with common-mode feedback, as depicted in Figure 13. The designed OPAMP exhibits 90-dB of closed loop gain and 80-degree of phase margin with 40-MHz of cutoff frequency. The diode of auto-

threshold control is implemented to diode-connected single NMOS transistor. Owing to the proposed ATC, the output of TIA exhibits only one operational amplifier. And the output of ATC doesn't exhibit resistive components. The proposed ATC can make easy the design of TIA and comparator circuits.

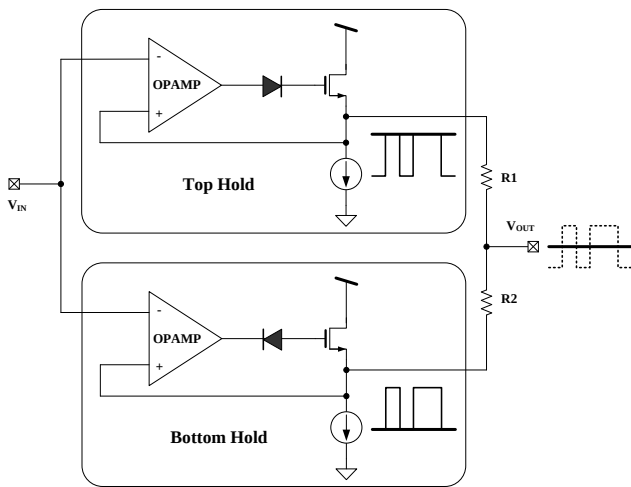


Figure 11. Conventional auto-threshold control block

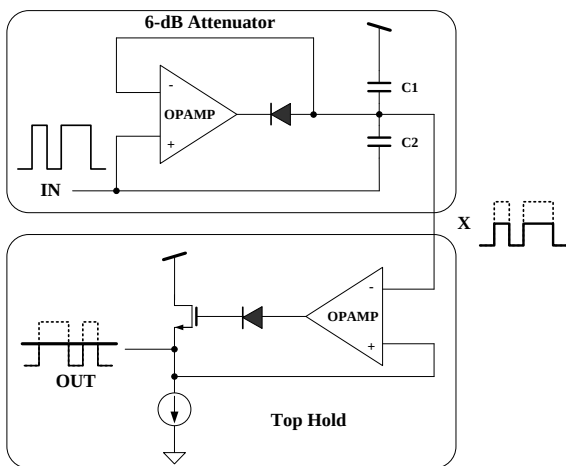


Figure 12. Proposed auto-threshold control block

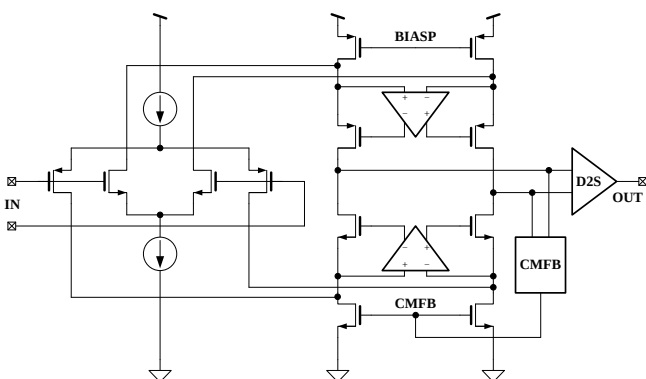


Figure 13. Gain-boosted folded-cascode operational amplifier

B. Post-layout Simulation Results

Figure 14 shows the transient response of the proposed FOR at 50-Mb/s PRBS and 200-nA of photo currents. The waveforms of the caption number #1 ~ #4 present the output of TIA, 6-dB attenuator, ATC, and output buffer, respectively. Despite of only 70-mV TIA output swing, the proposed ATC operates properly with only 2-mV of errors. And the final output of receiver depicts full digital level swing. The total receiver chip consumes only 2.8-mA DC currents at a 3.3-V single supply.

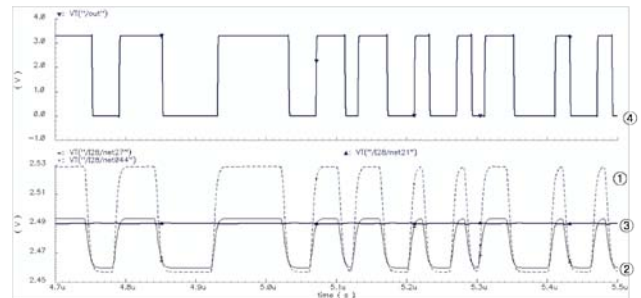


Figure 14. Transient response (@iPD=200-nA, 50-Mb/s PRBS31)

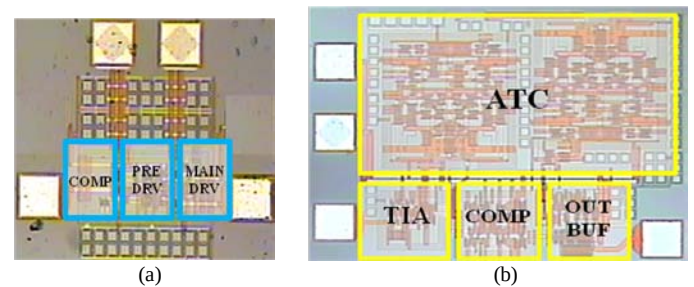


Figure 15. Chip microphotographies : (a) Fiber optic transmitter and (b) receiver

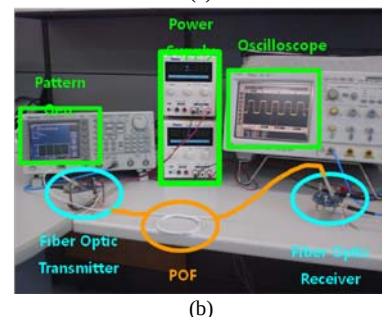
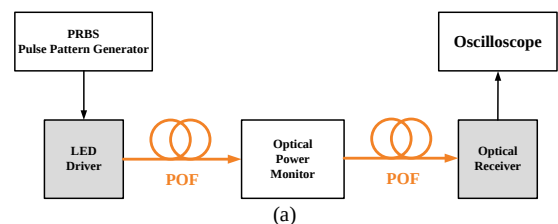


Figure 16. Measurement environment of POE Link : (a) Conceptual diagram and (b) real photograph

IV. MEASUREMENT RESULTS

The fiber optic transmitter and receiver for POF applications was fabricated and implemented using a low-cost 0.5- μm CMOS technology. Figure 15 shows the chip microphotography of the fabricated Fiber optic transmitter and receiver. The optoelectronics chipset occupies the area of 300- μm x 300- μm and 800- μm x 600- μm , respectively.

Figure 16 illustrates the conceptual block diagram and real photography of the measurement setup for POF optic link. The pulse pattern generator generates PRBS electrical signal, and that signal comes into FOT. The FOT drives off-chip 650-nm LED, and its optical power is measured and controlled by optical power monitor. The optical signal comes into FOR, and finally we can observe the digital level output signal, equals to input PRBS signal.

Figure 17 shows the measured pulse patterns according to data rates, from 1-Mb/s to 50-Mb/s for 27-1 PRBS pattern and -14-dBm of received optical power. The digital level output swing is guaranteed in the range of received optical power from -25-dBm to 0-dBm. However, for high-definition digital audio interface, under 5% of pulse-width distortion (PWD) errors is required. Therefore, the minimum optical power which meets the requirement of PWD is about -17.5-dBm, as shown in Figure 18.

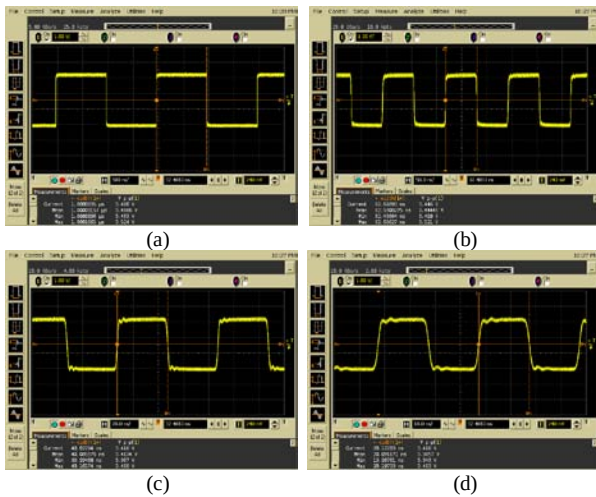


Figure 17. Measured waveform of POF link according to data rates : (a) 1-Mb/s, (b) 16-Mb/s, (c) 25-Mb/s, and (d) 50-Mb/s

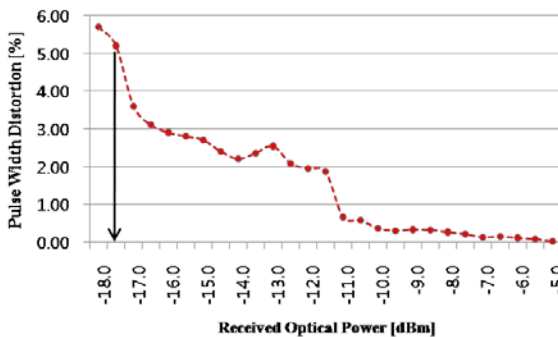


Figure 18. Pulse-width distortion according to received optical power (@50-Mb/s PRBS7)

V. CONCLUSION

Fiber optic transmitter and receiver for POF applications are designed and implemented using 0.5- μm CMOS technology. The designed FOT drives 650-nm LED having reliable and stable modulation current range from 3-mA to 4-mA against large supply voltage variation (2.6~3.6-V). And only 6-mA of currents is consumed including 3.5-mA of modulation current, while remaining 50-Mb/s of operating speed at a single 3.3-V supply voltage. Also, the proposed FOT occupies the area of 0.09- μm^2 . The FOR for POF has wide input dynamic range from 200-nA to 500-uA of incident photo currents. Therefore, various kinds of photo diodes can be exploited for proposed FOR, even CMOS-compatible integrated photo diode. Also, the FOR has wide operating frequency range from DC to 50-Mb/s. By satisfying wide frequency range, it is applied to various POF applications. The FOR exhibits only 2.8-mA of current consumption and 0.48- μm^2 . The measured sensitivity of FOR is about -25-dBm for 20% of PWD, and about -17.5-dBm for 5% of PWD, respectively.

Both the designed FOT and FOR operate from DC to 50-Mb/s of data rates and consume low power at a single 3.3-V supply voltage. Also, they have industry compatible pin description. Therefore, we expect the proposed FOT and FOR can be applied to various POF applications, such as high-definition digital audio interface, automotive networks, consumer electronics, and short reach optic communications.

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