

A 4-CH 10-Gb/s CMOS VCSEL Driver Array with Adaptive Optical Power Control

Won-Seok Oh ,Kang-Yeob Park, and Seonyoung Lee

Hybrid Signal Processing Research Center, Korea Electronics Technology Institute, Seongnam 463-816, Korea

oseok@keti.re.kr ,kpark@keti.re.kr, and drleesy@keti.re.kr

Abstract— In this paper, a 4-channel 10-Gb/s VCSEL driver array with adaptive optical power control is implemented using 0.13- μm CMOS technology. The proposed VCSEL driver compensates temperature effects of VCSEL using auto-power control (APC) and auto-modulation control (AMC). External monitoring photodiode (MPD) helps the detection of optical power and modulation. The proposed APC and AMC demonstrates 5~20-mA of bias-current control and 5~20-mA of modulation-current control, respectively. To enhance the bandwidth of the optical transmitter, active feedback amplifier with negative capacitance compensation is exploited. The whole chip consumes only 140-mW of DC power at a single 1.8-V supply under the maximum modulation and bias currents, and occupies the area of 1270- μm by 1080- μm excluding bonding pads.

Keywords— VCSEL Driver, Auto-Power Control, Auto-Modulation Control, Temperature Effects, CMOS

I. INTRODUCTION

Recently, data volume, speed and quality over display networks has rapidly grown, and thus it demands the development of high quality DVI and HDMI cables with ever-increasing transmission speed. Moreover, the interest about serialization of existing parallel cables requires more large data volume per line. Optical fibre is the most prime candidate as a medium of cable. Due to above reasons, the optic link can apply to not only comparative long distance display application, such as in-subway, in-airplane, in-vehicle networks, and so on, but also short distance video transmission, as shown in Figure 1.

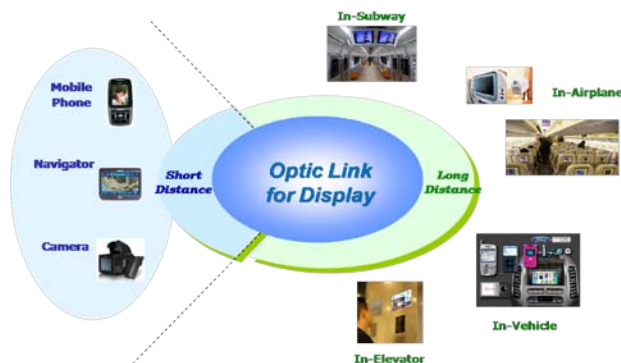


Figure 1. Application of optic link for display networks

Many researchers designing optical transmitter above 10-Gb/s of data rates implemented their designs using III-V compound semiconductors such as GaAs and InP that provide high bandwidth and good quality passive elements [1-3]. In low-cost and high volume short-haul applications around 10-Gb/s (such as LAN, MAN, chip-to-chip interconnection, and board-to-board interconnection), however, there has been an increasing interest in commercial deep-submicron CMOS technology. It is due to the unique advantages of CMOS technology, such as low power, low cost, good process maturity, and high integration capacity. Therefore, the objective of this paper is to investigate the possibility of implementing a high-speed CMOS optical transmitter for these cost-sensitive applications [4-9].

For almost semiconductor diodes, the junction voltage at fixed current decreases as the temperature increases. VCSELs are no exception, with approximately a $-2\text{-mV}/^\circ\text{C}$ variation. Figure 2 shows the conceptual I-P curve of the VCSEL according to the operating temperature. The slope efficiency falls off as the temperature increases, thus the modulated optical power decreases and the threshold current for the stimulated emission increases. To compensate these temperature-dependent variations, APC and AMC schemes are essential to maintain constant optical power, automatically.

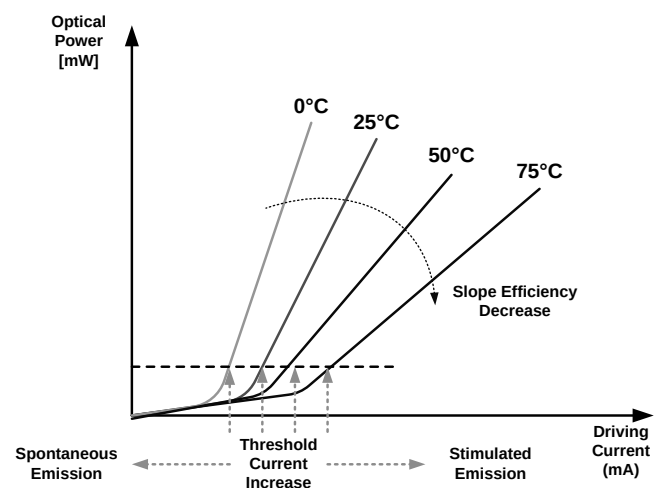


Figure 2. Conceptual I-P curve of VCSEL with respect to operating temperature

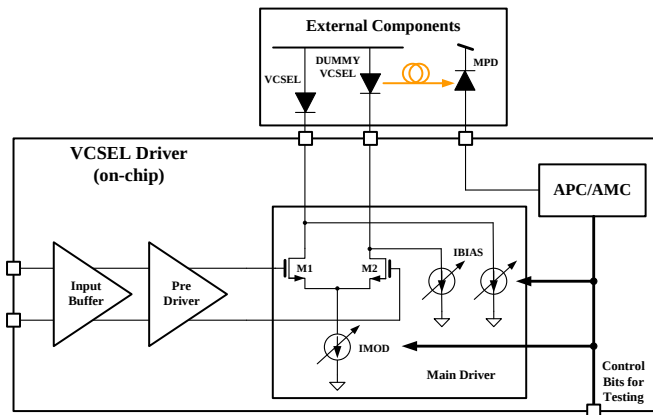


Figure 3. Proposed VCSEL Driver with Adaptive Optical Power Control

In this paper, a 4-channel 10-Gb/s VCSEL driver array with adaptive optical power control is designed and implemented in 0.13- μm CMOS technology. Section II describes the design details of the proposed VCSEL driver, especially APC and AMC schemes. In section III, the post-layout simulation results will be presented and analyzed. Finally, the conclusion is given by section IV.

II. PROPOSED VCSEL DRIVER

Figure 3 shows the proposed VCSEL driver with adaptive optical power control. Designed VCSEL driver consists of input buffer, pre driver, main driver and APC/AMC blocks. Two of VCSELs and monitoring photodiode (MPD) are externally implemented for the verification APC/AMC schemes.

A. Input Buffer and Pre Driver Design

Input Buffer has LVDS/CML compatible input configuration by adding center-tap control voltage (V_T) as shown in Figure 4. In conventional pre driver, the inductive peaking technique based on an active inductor, a LC-ladder filter network, or a series passive inductor, has been used to enhance the bandwidth. However, they suffer from several problems such as large die area, voltage headroom, and gain fluctuation. To solve these problems, we proposed a pre driver using active feedback and negative impedance compensation (NIC) as shown in Figure 5. Active feedback between two simple common-source amplifiers can improve gain-bandwidth product of the amplifier. A negative transconductance feedback, G_{mf} , returns a fraction of the output to the input of G_{m2} . Because this architecture doesn't resistively load the trans-impedance stage, thus the total bandwidth of the amplifier can be enhanced. However, intermediate node (X) between two common-source stages exhibits three active devices (G_{m1} , G_{m2} , and M_{F1}). Thus, this node is very capacitive. To compensate this parasitic capacitance, NIC stage is added at that point.

B. Main Driver Design

Figure 6 shows the block diagram of main driver with adaptive optical power control. Main driver drives VCSEL

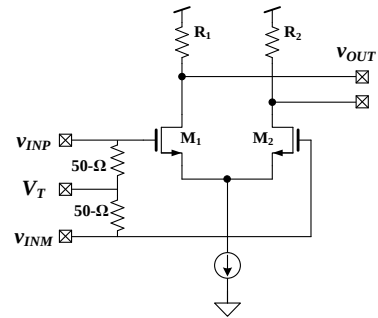


Figure 4. Schematic of Input Buffer

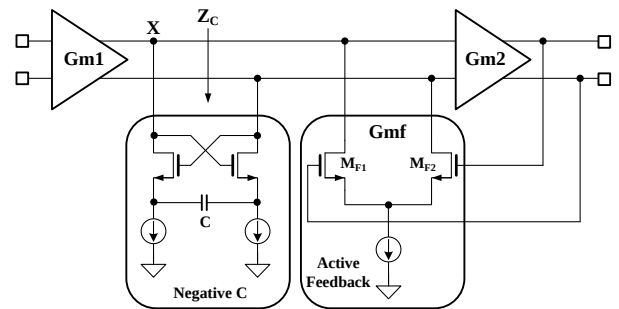


Figure 5. Schematic of Active Feedback Pre Driver with Negative Impedance Compensation

The detail APC and AMC scheme is presented in Figure 7. To compensate temperature effect, on-chip or off-chip APC and AMC are essentially required. To implement auto or adaptive control scheme, we need to detect the optical power or other corresponding parameters. We exploited monitoring photodiode (MPD) for the detection of optical power. MPD converts the optical power into electrical currents proportionally. The output of the MPD includes all information about AC and DC. Auto-power control scheme requires only DC information, namely the average optical power, while auto-modulation control scheme needs only AC information (the modulated power level). The output current of MPD is too small to handling. Thus the output of MPD converts and amplifies into voltage signal through trans-impedance amplifier (TIA). The peak detector, consisting of top hold and bottom hold circuit, extracts the peak values. The difference of the peak detector outputs means the AC information for auto-modulation control and the average of the peak detector outputs shows the DC information for auto-power control. Finally, we can get two DC levels including both AC and DC information of the optical output in virtue of operational amplifier (OPAMP). And these analog DC levels are converted to the several bits of digital code with the known reference levels for easy control by simple flash-type analog-to-digital converter, when the information returns to the optical transmitter. We

mapped the four digital codes to IBIAS and IMOD in 1-mA resolution per 1-LSB, thus we can control IBIAS and IMOD from default value to (default value + 15-mA). The default values of IBIAS and IMOD are 5-mA. In other words, we have the controllability 5~20-mA of IBIAS and 5~20-mA of IMOD, respectively. In this APC/AMC scheme, by simply adding the digital bits and the number of current source arrays, more precise and wide current control is possible.

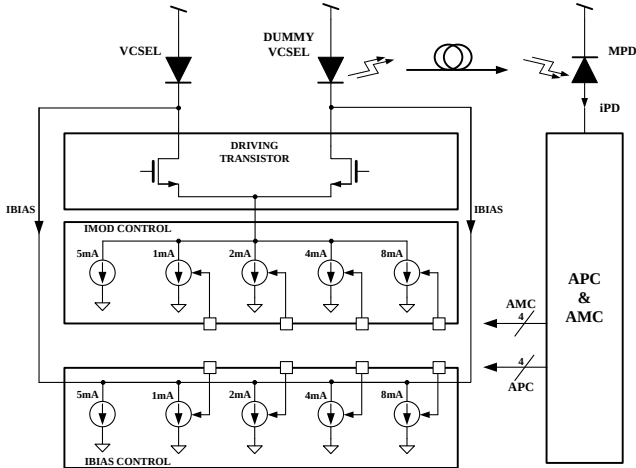


Figure 6. Main Driver with Adaptive Optical Power Control

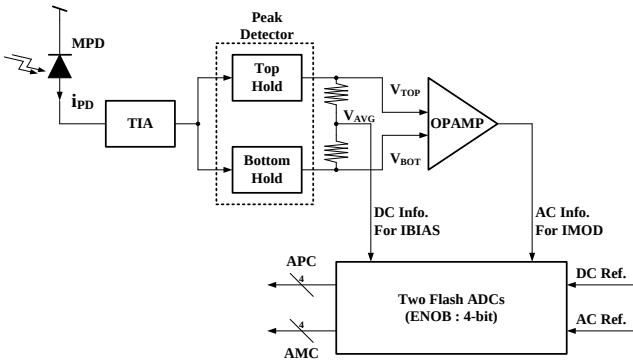


Figure 7. Detail Adaptive Optical Power Control Scheme

III. POST-LAYOUT SIMULATION RESULTS

The designed VCSEL driver has been fabricated in a standard 0.13- μm CMOS technology. The VCSEL driver operates in the frequency ranges from DC to 10-Gb/s at a 1.2-V supply. The chip area is 1.27-mm by 1.08-mm including ESD protected bonding pads. The chip layout of 4-channel VCSEL driver array is shown in Figure 8. The channel pitch is 250- μm , same to the pitch of commercial VCSEL array.

Pre driver is designed using active feedback amplifier with negative compensation. Figure 9 shows the simulated frequency response of the pre driver with and without active feedback and negative capacitance. Conventional two-stage common-source pre driver has 5.7-GHz of bandwidth. Active feedback pre driver exhibits 7.9-GHz, and active feedback pre driver using negative capacitance demonstrates 8.8-GHz of 3-dB bandwidth, respectively. The post-layout simulation results verify that the active feedback technique has 38% of bandwidth enhancement, and negative impedance compensation adds 11% of enhancement.

Figure 10 and 11 show the simulated 10-Gb/s eye patterns with auto-modulation control and auto-power control. The simulation results verify 5~20-mA of auto modulation control and 5-20-mA of auto bias control are possible. And the eye patterns with respect to the data rates from 1.25-Gb/s to 10-Gb/s are demonstrated in Figure 12.

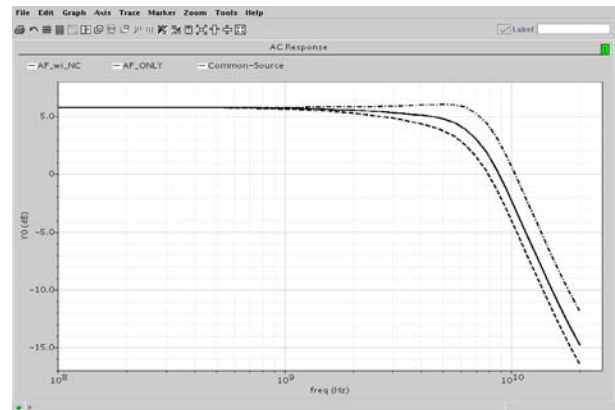


Figure 9. Simulated AC Response of Pre Driver

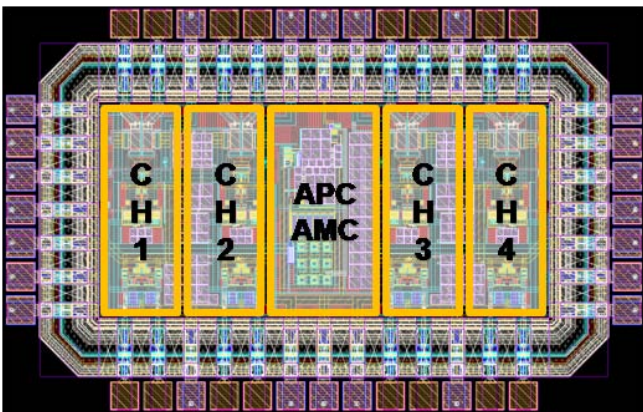


Figure 8. Chip Layout

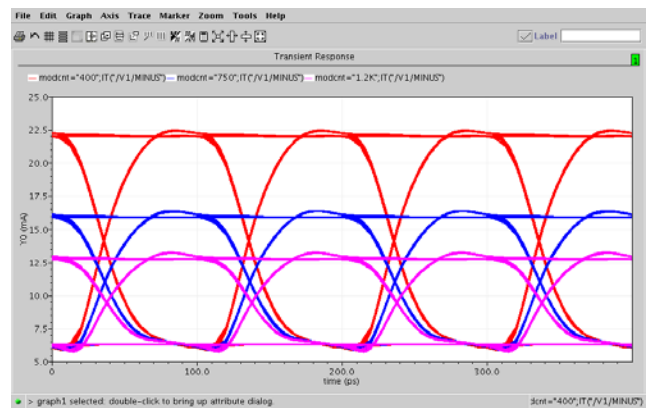


Figure 10. Simulated Eye Patterns with AMC (@10-Gb/s)

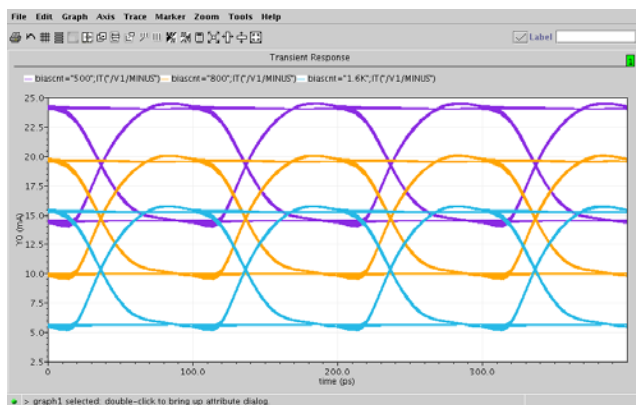
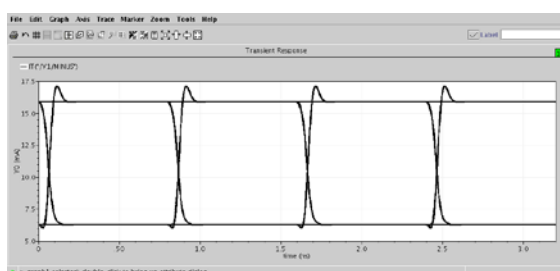
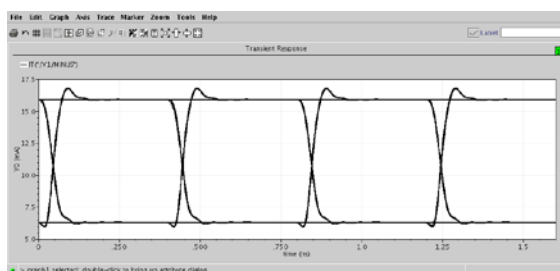


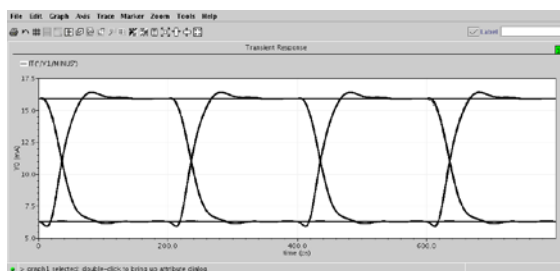
Figure 11. Simulated Eye Patterns with APC (@10-Gb/s)



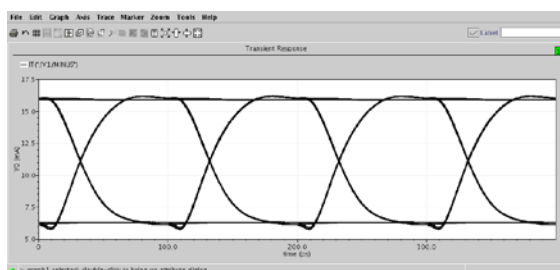
(a)



(b)



(c)



(d)

Figure 12. Simulated Eye Patterns with respect to the Data Rates : (a) 1.25-Gb/s, (b) 2.5-Gb/s, (c) 5-Gb/s, and (d) 10-Gb/s

IV. CONCLUSION

A 4-channel 10-Gb/s VCSEL driver with the proposed adaptive optical power control is designed and implemented in 0.13- μm CMOS technology. The performance of the proposed VCSEL driver is summarized in Table 1. The proposed adaptive optical power control loop properly operates with respect to the variation of the incident average and modulated optical power into monitoring photodiode. APC and AMC loop can control the bias and modulation current of the optical transmitter by the step of 1-mA and the total range of 15-mA. In the circuit level, to enhance the bandwidth of the pre driver, active feedback amplifier with negative capacitive compensation is proposed. The whole chip consumes 78-mA/channel of DC currents at a single 1.2-V supply under the maximum bias (20-mA) and modulation (20-mA) currents. Proposed CMOS VCSEL driver is expected to compensate successfully temperature effects of the VCSEL and provides cost-effective solution for short-haul multi-channel applications.

Table 1. Performance Summary of the 4-channel VCSEL driver

Technology	0.13- μm CMOS
Supply Voltage	1.2-V
Voltage Gain	10-dB
Bandwidth (-3dB)	8.4-GHz
VCSEL Max. Capacitance	< 0.5-pF
Adaptive Control Step	1-mA
APC/AMC Control Range	5~20-mA
Input Signal Format	CML/LVDS Compatible
Power Dissipation (4-ch)	374-mW
Chip Area	1.37-mm ²

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