

A Multichannel Downstream Receiver Supporting Channel Bonding in HFC Network

Jae-Ho Lee*, Dong-Joon Choi*, Soo-In Lee*, Whan-Woo Kim**

* Digital Broadcasting Research Division, ETRI, South Korea

** Chungnam National University, South Korea

jaehlee@etri.re.kr, djchoi@etri.re.kr, silee@etri.re.kr, wwkim@cnu.ac.kr

Abstract— In this paper, we propose a structure of a multichannel downstream receiver supporting four downstream channel bonding in hybrid fiber coax (HFC) networks. In addition, we show the implementation and measurement results. The structure we propose and implement consists of a radio frequency (RF) tuner and multichannel downstream receiver, which consists of a digital filter bank and four downstream demodulators. A downstream demodulator is comprised of a pre-forward error correction (pre-FEC) and FEC decoder. We simulate a bit error rate (BER) of the pre-FEC with a fixed precision. The simulation results show that the required E_b/N_0 is 18 dB when the BER of 64QAM is 10^{-5} and the required E_b/N_0 is 23 dB when the BER of 256QAM is 10^{-5} . The proposed multichannel downstream receiver is implemented with field programmable gate array (FPGA) and ASIC using 0.18 μm CMOS technology with a supply voltage of 1.8 V.

Keywords— DOCSIS 3.0, downstream channel bonding, HFC, multichannel downstream receiver, FEC, RF tuner

I. INTRODUCTION

The demands for high-speed data rate over hybrid fiber coax (HFC) downstream are increasing to serve a triple service including broadcasting, data and voice. For satisfying these needs, CableLabs, which is a cable standard organization of the United States, announced the data over cable service interface specifications (DOCSIS) 3.0 in 2006. Cable system is comprised of cable modem termination system (CMTS) in headend and cable modems (CMs) in cable subscribers which are connected with HFC. A downstream transmitter in CMTS transmits QAM modulated signal through downstream that has a 6MHz bandwidth. According to DOCSIS 3.0, CM receiver must receive at least 4 downstream channels simultaneously, located independently within an arbitrary 60 MHz window in the downstream frequency band [1]. This method is referred to channel bonding, which is similar to frequency division multiplexing (FDM).

In this paper, we propose a structure of a multichannel downstream receiver supporting 4 downstream channel bonding. A multichannel downstream receiver has a digital filter bank and 4 downstream demodulators which are composed of pre-forward error correction (pre-FEC) and FEC.

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And, we find the bit error rates (BER) of 64QAM and 256QAM with computer simulation. In addition, we implement a multichannel downstream receiver with FPGA for prototype, and we also implement the multichannel downstream receiver using 0.18 μm CMOS technology with a supply voltage of 1.8 V.

II. PROPOSED MULTICHANNEL DOWNSTREAM RECEIVER

First, we introduce the parameters of downstream transmitter listed in the DOCSIS 3.0 specification briefly. And then, we explain a structure of a multichannel CM receiver supporting at least four downstream channels. Finally, we show the computer simulation and measurement results of pre-FEC with 64QAM and 256QAM.

A. DOCSIS 3.0 Specification

DOCSIS 3.0 adopted the ITU-T J.83 annex B as the standard of downstream transmission. The block diagram of transmitter is shown in Figure 1 and the parameters are listed in Table 1 [2].

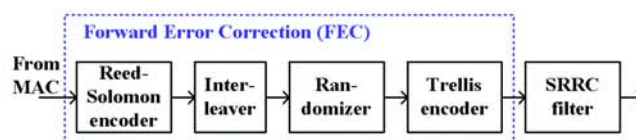


Figure 1. A block diagram of downstream transmitter.

TABLE 1. PARAMETERS OF DOWNSTREAM TRANSMITTER

RS encoder	(128, 122) code over GF(128) for 64QAM and 256QAM
Interleaver	Convolutional Interleaver
Randomizer	Polynomial : $f(x) = x^3 + x + a^3$
TCM encoder	4/5 puncturing
Symbol rate	5.056941 Mbaud for 64-QAM 5.360537 Mbaud for 256-QAM
Bandwidth	6MHz for 64QAM and 256QAM
Roll-off factor of SRRC filter	0.18 for 64QAM 0.12 for 256QAM

As shown in Figure 1, Reed-Solomon encoder is used as an outer code and provides block encoding and decoding to correct up to three symbols within one RS block. In addition, Trellis encoder is used as an inner code and provides

convolutional encoding and decoding with the possibility of using soft decision trellis decoding of errors.

B. Multichannel downstream Receiver supporting four downstream channel bonding

Figure 2 shows the proposed multichannel downstream receiver supporting four downstream channel bonding.

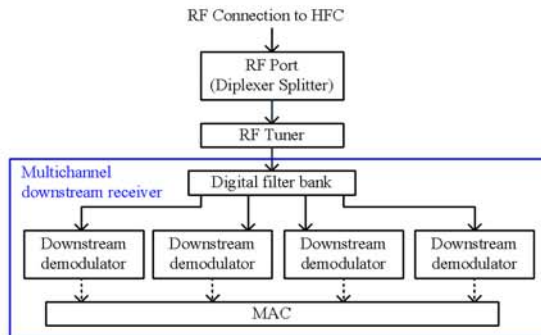


Figure 2. Proposed multichannel downstream receiver.

As shown in Figure 2, the multichannel downstream receiver consists of a digital filter bank and four downstream demodulators. A diplexer splitter is used to split channel between downstream channel and upstream channel. The total input bandwidth of RF tuner is 24MHz, and the center intermediate frequency (IF) of RF tuner output is 33MHz.

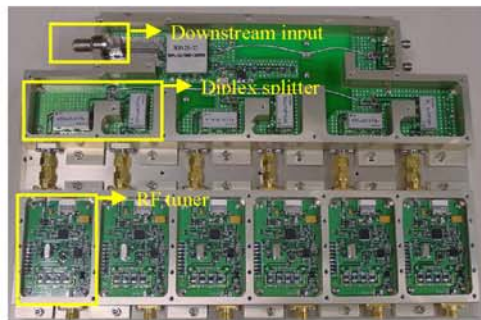


Figure 3. An implemented RF tuner.

As shown in Figure 3, 6 RF tuners are implemented to receive 4 downstream channel bonding, located independently within an arbitrary 60 MHz window in the downstream frequency band and each RF tuner has the ability to tune four downstream channels with 24 MHz bandwidth.

Figure 4 shows the signal flow between RF tuner output and a digital filter bank [3].

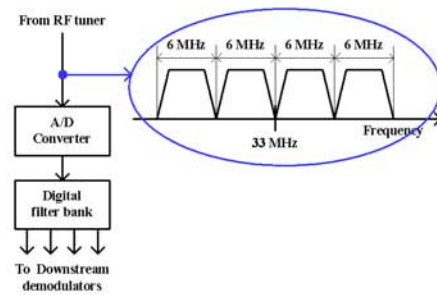


Figure 4. Input and output of digital filter bank.

As shown in Figure 4, four downstream signals centered at 33MHz IF are converted into digital signals, which are down-converted to baseband signals centered at zero frequency.

Figure 5 shows the downstream demodulator which consists of pre-FEC and FEC.

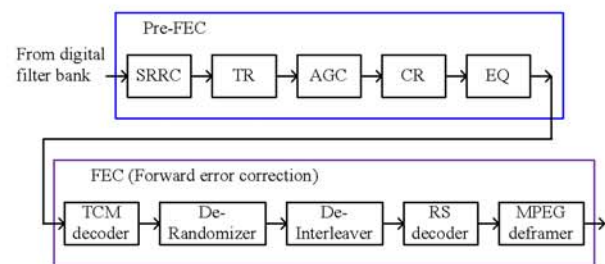


Figure 5. Downstream demodulator.

A pre-FEC consists of a timing recovery (TR), an automatic gain control (AGC), a carrier recovery (CR) and an equalizer (EQ). TR compensates A/D converter sampling clock jitter [4]. AGC compensates signal's magnitude [5]. CR estimates and compensates a frequency offset caused by local oscillators between a transmitter and a receiver [6]. EQ compensates the channel distortion with feed forward filter using least mean square (LMS) algorithm [7], [8], [9].

FEC consists of TCM decoder, derandomizer, deinterleaver, and RS decoder. MPEG deframer recovers the sync byte of MPEG-2 TS.

C. Results of simulation and measurement

We simulate the BER performance of pre-FEC with the conditions having a frequency offset, and a phase offset, and a timing offset, and multi-path channel in case of the floating point and the fixed point individually as shown in Figure 6 and 7, respectively.

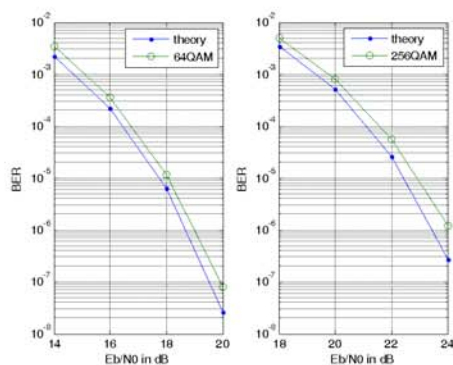


Figure 6. BER of 64QAM and 256QAM with floating point.

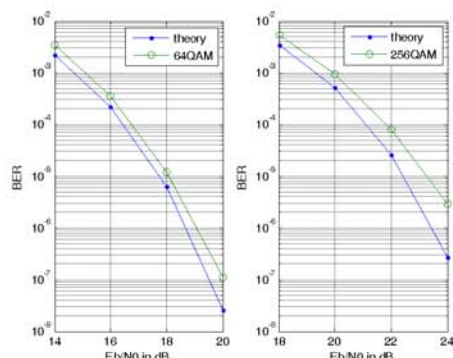


Figure 7. BER of 64QAM and 256QAM with fixed point.

As can be seen in Figure 7 and 8, there is no difference of E_b/N_0 at BER of 10^{-4} between floating point and fixed point in case of 64QAM. But, there is 0.3 dB E_b/N_0 loss at BER of 10^{-4} between floating point and fixed point in case of 256QAM.

On the basis of simulation results, we implement a digital filter bank and four downstream demodulators with FPGAs as shown in Figure 8. Table 2 lists the bit resolutions of interfaces between the internal modules in FPGAs.

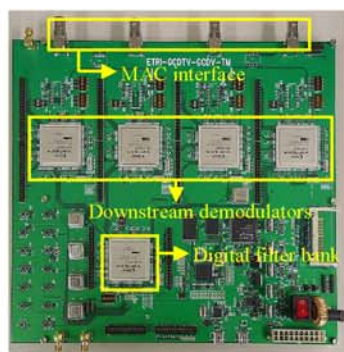


Figure 8. Implemented digital filter bank and downstream demodulators.

TABLE 2. BIT RESOLUTION OF INTERNAL MODULE INTERFACE

Internal module	Bit resolution (bits)
A/D converter	14
TR	<12,3,t>
AGC	<12,2,t>

CR	<12,2,t>
EQ	<8,3,t>
RS decoder	7
MPEG deframer	8

As listed in Table 2, the <12,3,t> of TR means that the total bits are 12 bits, 3 bits among them are integer bits and t is the 2's complement.

Figure 9 shows the test bed for receiving four downstream channels simultaneously. Four bonded downstream channels transmit MPEG-2 TS stream as source data. RF center frequencies of downstream channels are located at 699MHz, 705MHz, 711MHz and 716MHz individually as shown in Figure 10. RF tuner converts the downstream channels to IF frequencies as shown in Figure 11. The IF center frequencies are located at 24MHz, 30MHz, 36MHz and 42MHz individually. A/D converter performs sampling, and digital filter bank converts IF downstream channels to baseband signals, and downstream demodulators detect the transmitted MPEG-2 TS stream. We confirm the MPEG-2 TS is screened in TV without errors.

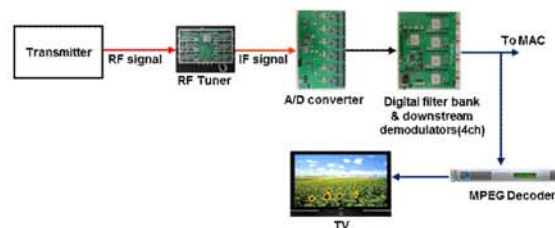


Figure 9. Test bed for multichannel downstream receiver.

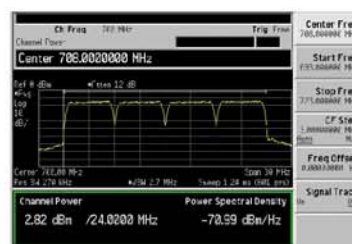


Figure 10. RF spectrum of 4 downstream channel bonding.

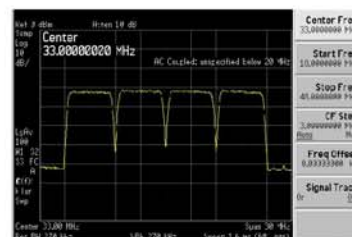


Figure 11. IF spectrum of 4 downstream channel bonding.

Figure 12 and 13, respectively, show the constellations of EQ outputs, captured from FPGA, in case of 64QAM and 256QAM for one downstream channel. In addition, we confirm the result of constellation is the same as the other channels.

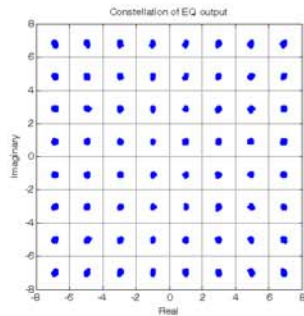


Figure 12. Constellation of 64QAM.

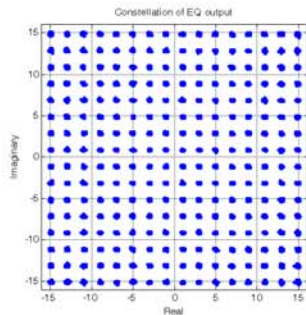


Figure 13. Constellation of 256QAM.

After we confirm the operation of digital filter bank and downstream receivers, we implement the digital filter bank and downstream receivers using 0.18 μm CMOS technology with a supply voltage of 1.8 V. A board mounted with ASIC chip, shown in Figure 14, is under test.

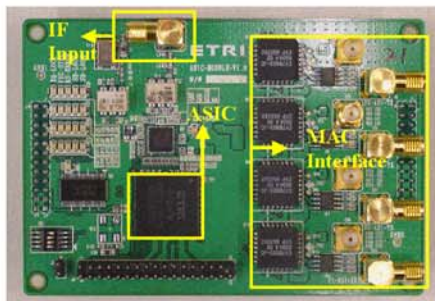


Figure 14. ASIC board under test.

III. CONCLUSION

DOCSIS 3.0 specification adopts channel bonding for broadband multimedia service.

In this paper, we propose a structure of a multichannel downstream receiver to support four downstream channel bonding and simulate the BER performance of pre-FEC. When the BER of 64QAM is 10^{-5} , the required E_b/N_0 is 18 dB. When the BER of 256QAM is 10^{-5} , the required E_b/N_0 is 23 dB. In addition, we implement a multichannel downstream receiver with FPGA and ASIC.

The proposed structure and implemented ASIC of multichannel downstream receiver are expected to be

applicable for supporting DOCSIS 3.0 downstream channel bonding.

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