

High Inductance LTCC Based Spiral Inductor with Small Area and High Quality Factor

Ikechi Augustine Ukaegbu*, Kwang-Seong Choi**, Jamshid Sangirov*, Tae-Woo Lee*, and Hyo-Hoon Park*

*Department of Electrical Engineering, Korea Advanced Institute of Science & Technology (KAIST),
119 Munjiro, Yuseong-Gu, Daejeon, 305-732, Korea

**Electronics and Telecommunications Research Institute (ETRI),
161 Gajeong-dong, Yuseong-gu, Daejeon 305700, Korea
aus20@kaist.ac.kr

Abstract—In this paper, the characterization of spiral inductors and the design of a novel spiral inductor based on low temperature co-fired ceramics (LTCC) is described. Due to the semi-stacked nature of the inductor, a peak quality factor ($Q_{\max}$) of 43.3 and an effective inductance L_{eff} of 14.41 nH has been obtained. Our novel spiral inductor occupies a smaller area when compared with the conventional planar inductor of similar inductance.

Keywords—Semi-stacked spiral inductor, LTCC, quality factor, self resonance frequency, inductance.

I. INTRODUCTION

There is a continuous need for increasing the packaging density in radio frequency (RF) devices leading to continuous interest and research in the development of materials, their design and manufacturing techniques. It is well known that inductors occupy large space in radio frequency integrated circuits (RFICs). Therefore, in inductor design, it is important to reduce the area occupied.

Spiral inductors are important components of RF circuits such as RF amplifiers, impedance matching networks and voltage-controlled oscillators (VCOs) [1]. Some RF front-end building blocks such as power amplifier often require off-chip matching and biasing components [2], [3], since it is difficult to accommodate them on-chip due to their Q factor and current handling capability limitation. Low temperature co-fired ceramics (LTCC) technology offers one of the solutions to this due to its packaging capabilities.

In inductor design, quality factor (Q) and self resonance frequency (F_{self}) are the two most important parameters of the spiral inductor [4], [5]. Therefore in inductor design, it is important to enhance the Q and F_{self} of an inductor in a small area by lowering parasitic effects such as skin effect, coupling capacitance and line resistance. In order to improve the performance of spiral inductors, many approaches have been applied. Thick metal or stacked layers can increase the Q factor by reducing the metal losses (series resistance) [6]

and by reducing the number and area of overlapping layers; the F_{self} can be improved by reducing parasitic capacitance. It is difficult to improve Q and F_{self} at the same time. Thus the designer is faced with making trade-offs between performance (Q , F_{self}), inductance (L), and area.

By taking the advantage of the multilevel interconnects available and shunting several metal layers, an effective thicker metal is achieved which helps to reduce inductor loss [6], [7]. The simple stacked spiral inductor structure [8] with vertical series of monolayer-spiral inductors is an effective way of achieving smaller inductor area but this comes at the expense of degrading the F_{self} as a result of the parasitic capacitance between the upper and lower metal lines.

Sometimes it is difficult to design inductors with high inductance while still maintaining a high Q -factor and F_{self} within a small area. Therefore, in this paper, we propose a novel small area high inductance semi-stacked spiral inductor structure with high Q factor.

Three single-ended spiral inductors have been fabricated and characterized in order to validate the proposed inductor structure.

II. Q FACTOR DEFINITIONS AND INDUCTOR MODEL

A. Q factor definitions

The quality factor, Q of an inductor constitutes a very important figure of merit in discussing the performance of spiral inductor. The quality factor is defined as

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy in one cycle}} \quad (1)$$

Two different definitions are often used for an inductor's Q factor which basically depends on how we define the energy stored. Equation (1) also defines the Q factor of an LC tank. For an inductor, the energy stored in the magnetic field is of

more importance than the energy stored in the electric field as parasitic capacitances. This Q factor can be represented as Q_L as shown in (2).

$$Q_L = 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one cycle}} \quad (2)$$

Which can be obtained from measurements to be:

$$Q_L = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})}, \quad (3)$$

where Y_{11} and Z_{11} represent the admittance and impedance of the inductor, respectively, when one terminal is connected to the ground [9], [10]. Im and Re respectively represent the imaginary and real components of the admittance or impedance.

B. Inductor Model

The inductor model consists of three different spiral inductors with two and half (2.5), three and half (3.5), and four and half (4.5) turns respectively. The inductors have three different line widths with a constant spacing of 0.16 mm. They have two layers with the second layer used for the under-pass. Fig. 1 shows a high frequency two-port electrical model of inductors based on LTCC [11].

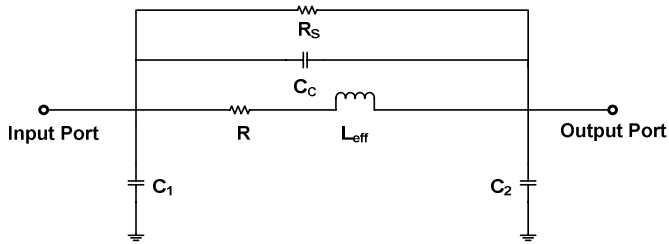


Figure 1. Two-port electrical model of LTCC inductors

From Figure 1, L_{eff} models the effective inductance; R models the loss in the metal lines (which is also the real part of the series impedance of an inductor); C_1 and C_2 are the combined coupling effect between the port pads and ground plane, and also between the inductor lines and the ground plane; C_s is the coupling capacitance between the inductor lines and the underpass and between neighboring (adjacent) inductor lines. R_s models the resistance due to skin effect at very high frequencies. At low frequencies, this can be neglected in the model. One way to increase the effective inductance, L_{eff} is by moving the ground plane far from the inductor plane [12], thereby reducing the shunt parasitic capacitances, C_1 and C_2 . Keeping the ground plane close to the inductor plane reduces L_{eff} due to the negative mutual

coupling caused by the current flowing in the ground plane in the opposite direction which is in the opposite direction to the current flowing in the inductor [13]. Figure 2 shows the photograph of three fabricated inductor structures which were measured to obtain their L_{eff} , Q_L , and F_{self} . Further, keeping the inductor plane on the surface layer helps to minimize dielectric loss by maintaining part of the inductor field propagating in the air [12].

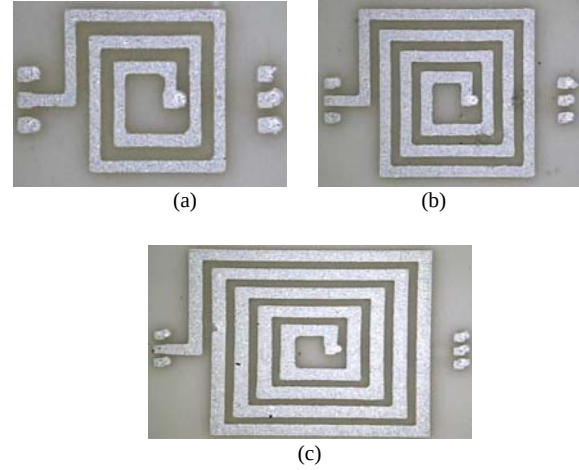
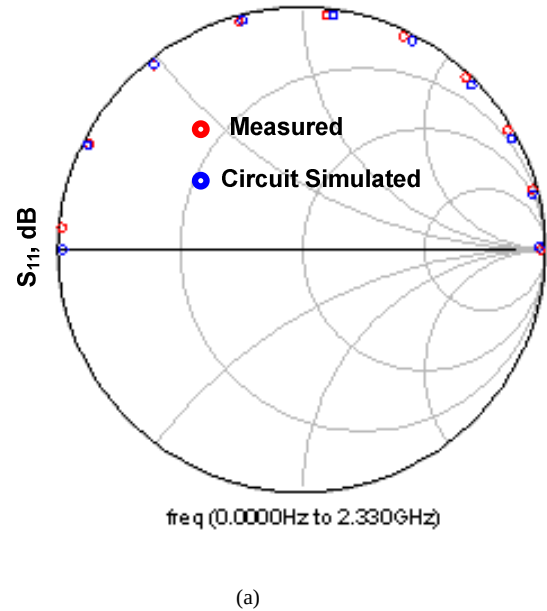


Figure 2. Photographs of the fabricated (a) 2.5 turns (b) 3.5 turns, and (c) 4.5 turns inductor structures

Figure 3, Figure 4, and Figure 5 show the measured and simulated S-parameters and quality factors of the three fabricated planar inductor test structures.



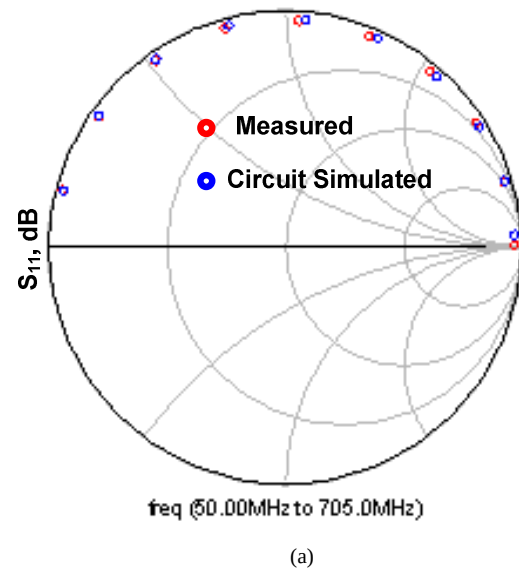
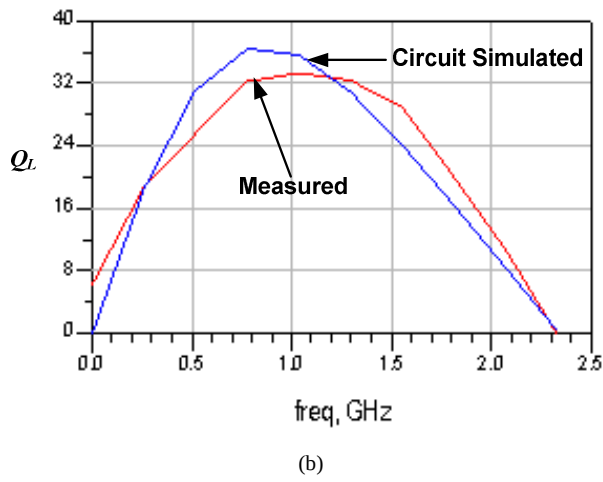


Figure 3. Measured and modeled (a) S-parameters and (b) quality factors of the 2.5 turns inductor

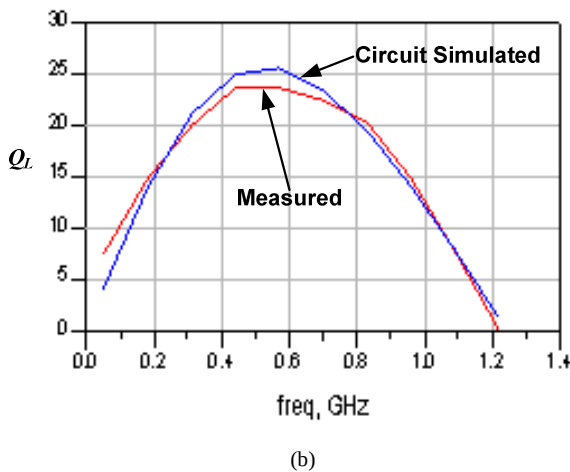
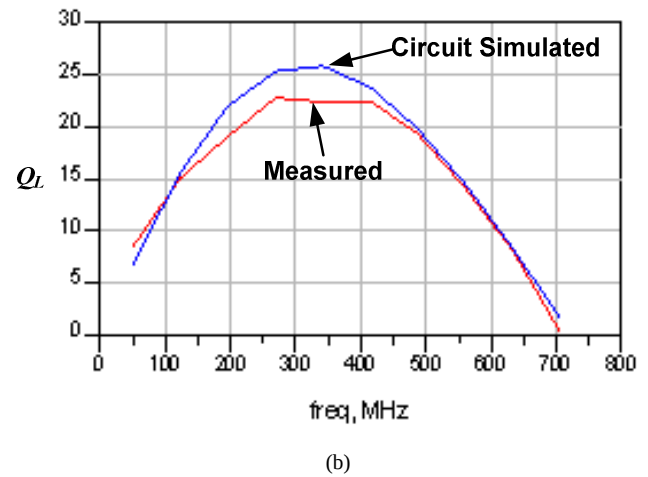
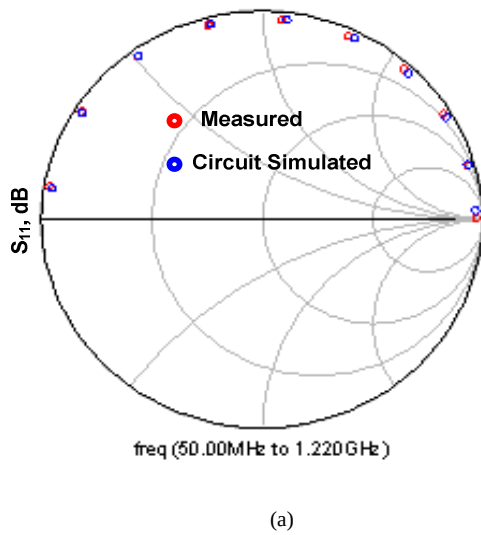


Figure 5. Measured and modeled (a) S-parameters and (b) quality factors of the 4.5 turns inductor

The three inductor structures occupy a surface area of 1.93 mm x 3.61 mm, 2.9 mm x 4.39 mm, and 4.06 mm x 5.6 mm respectively. The values of L_{eff} , R , C_1 , C_2 , F_{self} , and Q_L for the 2.5 turns inductor are 7.15 nH, 0.59 Ω , 0.55 pF, 0.11 pF, 2.33 GHz, and 33.5 respectively and for the 3.5 turns inductor are 12.4 nH, 0.95 Ω , 1.2 pF, 0.12 pF, 1.22 GHz, and 23.1 respectively. The values of the extracted model parameters for the 4.5 turns inductor are 20 nH, 0.94 Ω , 2.43 pF, 0.11 pF, 0.71 GHz, and 22.7 respectively for L_{eff} , R , C_1 , C_2 , F_{self} , and Q_L . Some parameters that influence the behavior and performance of inductors include the number of turns, N , the width of the coils or metal lines, W , the inner radius of the spiral inductor, R_{in} , and the distance between the inductor and the ground plane, d [14]. Some of these factors are illustrated in Figure 6.

Figure 4. Measured and modeled (a) S-parameters and (b) quality factors of the 3.5 turns inductor

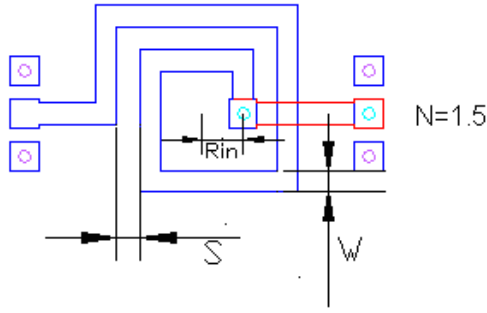


Figure 6. An inductor model showing the parameters that influence the performance of an inductor

A higher quality factor was noticed with the 2.5 turns inductor when compared to the 3.5 turns and 4.5 turns. The increasing number of turns increases inductance since the total inductor length increases as shown in Figure 7.

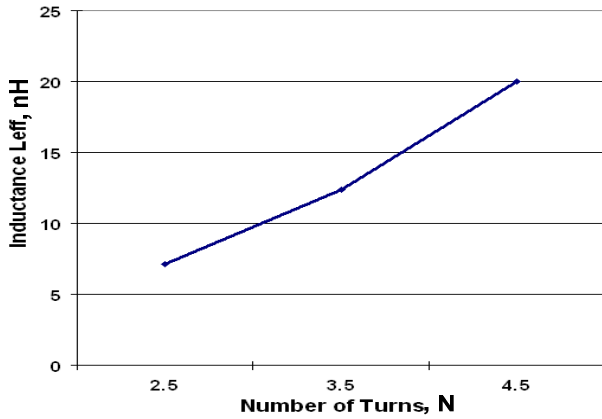


Figure 7. The effect of increasing the number of turns, N and width, W on the inductance of the inductor

The inductance of an inductor is directly proportional to its length but inversely proportional to the line width as in (4) [14].

$$L = \frac{\mu_0 l}{2\pi} \left(\ln \frac{2l}{\rho} - 1 \right), \quad (4)$$

where d is the distance between the inductor plane and the ground plane, w is the line width, l is the metal length, μ is the permeability of the medium, and ρ is a function of length, width and metal thickness. Increase in the number of turns gives rise to a larger rate of increase in the inductance than the effect of increasing the width. At lower frequencies, the quality factor of the inductor with a larger number of turns has almost the same value as that of a lower number of turns as in Figure 8. This is as a result of reduced series resistance due to increased line width. At higher frequencies, parasitic capacitance and frequency dependent resistance come into play, which tends to have more effect on the inductor with larger turns and degrades the quality factor. Inductors with lower number of turns have lower series resistance, lower

parasitic capacitance, and hence higher Q_L at high frequencies.

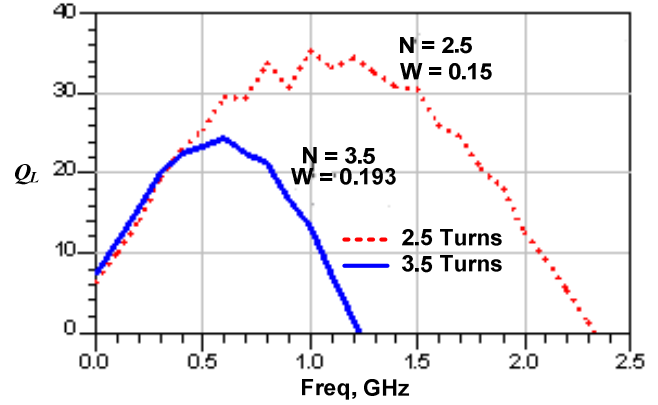


Figure 8. The influence of number of turns, N and increasing metal width, W for spiral inductors with same spacing, S of 0.16 mm

The spacing S between inductor metal lines also plays a role in the performance of an inductor. A larger spacing with other parameter constants (N , W , and R_{in}) brings about an increase in the inductance. This is due to the fact that as spacing increases, the total length of the inductor increases which gives rise to more amount of magnetic flux density and hence a higher inductance. Larger spacing also lowers the coupling parasitic capacitance between the inductor lines. Inductors with higher R_{in} have higher inductance when compared to those with smaller R_{in} . Magnetic field intensity reaches its maximum at the center of the spiral inductor and thus for inductors with full inner windings (small R_{in}), a large portion of the magnetic field passes through the inner metal turns thereby inducing in the metal turns a strong current density, and thus increasing their resistivity [13].

III. THE SEMI-STACKED SPIRAL INDUCTOR

The geometry of the semi-stacked spiral inductor is shown in Figure 9. It has three turns with the outermost and innermost turns on the top layer. The second turn is embedded in the second layer, occupying the space between the outermost and innermost turns. The semi-stacked structure is designed in such a way that the turn in the second layer does not overlap with turns on the top layer. Thus, the inter-wire capacitance as well as the underpass capacitance is significantly reduced [15].

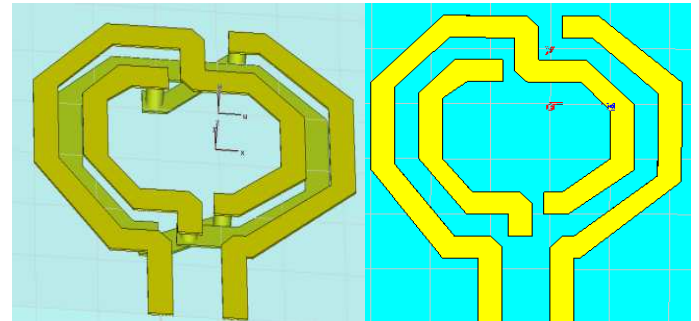


Figure 9. 3-D view and top view of the three-turn semi-stacked spiral inductor

This architecture takes the advantage of multiple mutual inductance which occur in the 3-D structure by reducing the area consumed (by up to 45%) when compared to conventional spiral inductors. Figure 10 shows the S-parameters of the semi-stacked spiral inductor structure.



Figure 10. S-parameters of the semi-stacked spiral inductor structure

The area improvement does not come at the expense of inductor performance. Also the longest turn is located on the top layer with the lowest resistivity can lower the resistance of the inductor, which will in turn reduce the amount of degradation in the Q-factor. The spacing between the adjacent turns in the semi-stacked inductor structure can be minimized to zero thereby consuming a smaller area than conventional inductors of the same inductance. This also increases the mutual and self inductance of an inductor and thus increases the total inductance of the inductor. The inductor was designed in an LTCC substrate with dielectric constant, ϵ_r of 8.4. The metal lines have a thickness of 12 μm with line width of 200 μm and inter-layer (between the top and second layers) gap of 100 μm . Table 1 shows a comparison of the result of the three-turn semi-stacked inductor structure with conventional stacked and planar structures.

TABLE 1. SUMMARY OF COMPARED RESULTS OBTAINED FROM THREE LTCC BASED INDUCTOR STRUCTURES

Parameter	Semi-stacked (N=3)	Conventional stacked (N=3)	Planar (N=3)
F_{Self} (GHz)	1.83	1.32	1.75
Q_L	43.3	47.4	42.1
L_{eff} (nH)	14.41	22.8	14.33
Surface Area (mm)	1.11 x 1.5	2.3 x 1.8	2.3 x 2.08

The semi-stacked inductor structure showed a higher F_{self} and quite a high inductance while still maintaining the smallest surface area possible.

IV. CONCLUSIONS

Three inductor structures were fabricated and characterized. Some of the factors that influence the

performance of an inductor such as the number of turns, N , the width of the coils or metal lines, W , the inner radius of the spiral inductor, R_{in} , and the distance between the inductor and the ground plane, d have all been described. Furthermore, a semi-stacked inductor structure with high inductance value has been designed which give a better performance and occupies a smaller surface area when compared with other inductor structures of the same number of turns and the same inductance value (for the case of planar type). The inductor library can be applied in RF monolithic microwave integrated circuits (MMICs) and high speed ICs.

ACKNOWLEDGMENT

This work was supported by the New IT Project for global competitiveness strengthening of the advanced mobile devices and equipments of the Chungcheong Leading Industry Office of the Korean Ministry of Knowledge Economy (MKE).

REFERENCES

- [1] Y.-Yang and Z.-F. Li, "Group-cross symmetrical inductor (GCSI): A new inductor structure with higher self-resonance frequency and Q factor," in *IEEE Trans. Magn.*, vol. 42, No. 6, pp. 1681–1686, June 2006.
- [2] P. Tseng, G. Yang, G. yang, and M. F. Chang, "3-V monolithic SiGe HBT power amplifier for dual-mode (CDMA/AMPS) cellular handset applications," *IEEE J. Solid-state circuits*, vol. 34, pp. 1338–1344, sept 2000.
- [3] K. C. Tsai and P. Gray, "1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," *IEEE J. Solid-state circuits*, vol. 34, pp. 962–967, Mar. 1999.
- [4] C. Y. Kim, H. J. Kim, and J. R. Kim, "An integrated LTCC inductor," *IEEE Trans. Magn.*, vol. 41 No. 10, pp.3556 – 3558, oct. 2005.
- [5] K. Sugahara, S. Tanabe, and M. Yamaguchi, "Frequency-independent equivalent circuit model for ferromagnetic RF integrated inductors," *IEEE Trans. Magn.*, vol. 41 No. 10, pp.3529 – 3551, oct. 2005.
- [6] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microw. Theory Tech.*, vol. 44, No. 1, pp. 100–104, Jan. 1996.
- [7] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Integrated RF and microwave components in BiCMOS technology," *IEEE Trans. On Elec. Devices*, vol. 43. No. 9, Sept. 1996.
- [8] K. Hijioka, A. Tanabe, H. Ohtake, T. Onodera, and Y. Hayashi, "Low-loss LSI interconnects on novel "partially low-k plugged Si substrate" (PLP-Sub) for RF/ubiquitous applications," *IEEE int. Interconnect Tech. Conf.*, p.60, 2006.
- [9] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RFIC's," *IEEE J. Solid-state Circuits*, vol. 33, pp. 1470–1481, 1998.
- [10] A. M. Niknejad and R. G. Meyer, "Analysis, design and optimization of spiral inductors and transformers for Si RF IC's," *IEEE J. Solid-state Circuits*, vol. 33, pp. 743–752, Aug. 1987.
- [11] I.A. Ukaegbu and K.S. Choi, "Report on inductor analysis for LTCC based RF passive library," *ETRI project report*, Oct. 2008.
- [12] A. Sutono, D. Heo, Y. E. Chen, and J. Laskar, "High-Q LTCC-based passive library for wireless system-on-package (SOP) module development," *IEEE Trans. Microw. Theory Tech.*, vol. 49, No. 10, pp. 1715–1724, Oct. 2001.
- [13] J. Aguilera and R. Berenguer, "Design and test of integrated inductors for RF applications," *Kluwer academic publishers*, 2003.
- [14] R. K. Ulrich and L. W. Schaper, "Integrated passive component technology," *John Wiley & Sons, Inc., publication*, 2003.
- [15] K. Kang, J. Shi, S. C Rustagi, L.-W. Li, K. Mouthaan, A.-Y. Yin, and S. Zouhdi, "On-chip vertically tapered solenoid inductor with high self-resonance frequency," *IET Elec. Let.*, vol. 43, No. 16, Aug. 2007.