

A Low-Power Current-Reused Folded Cascode Harmonic Rejection Mixer for DVB-T Tuner

Chang-Jin JEONG, Yang SUN, Dae-Young YOON, Sok-Kyun HAN, Sang-Gug LEE

Department of Electrical Engineering,
KAIST (Korea Advanced Institute of Science and Technology),
119, Mujiro, Yuseong-gu, Daejeon, Republic of Korea

ichj@kaist.ac.kr, yixiusky@kaist.ac.kr, dyyoon07@kaist.ac.kr, sskk@kaist.ac.kr, sglee@ee.kaist.ac.kr

Abstract—In this paper, a novel low-power current-reused folded cascode harmonic rejection mixer (HRM) for digital video broadcasting-terrestrial (DVB-T) tuner application is proposed. In proposed architecture, by adopting current-reused folded cascode topology, linearity of the HRM is improved and the low-power implementation is realized. In the frequency range of 48~862 MHz, simulation results of the proposed HRM show 41.1~41.5 dB 3rd-order harmonic rejection ratio, 6~9.9 dB voltage gain, 10.9~11.3 dB NF, and 5.3~9.8 dBm IIP3, while drawing 1.5 mA current from a 1.2 V supply in a standard 0.13 μ m CMOS technology.

Keywords—Mixer, Harmonic Rejection Mixer, Current Reused, Harmonic Rejection, DVB-T, Tuner

I. INTRODUCTION

Recently, the use of digital TV (DTV) is expected to be rapidly increased in the future. Today's digital TV standards, such as ATSC (Advanced Television Systems Committee) and DVB-T (Digital Video Broadcasting-Terrestrial), cover a wide frequency range from 48 to 862 MHz. Therefore, there are many challenging technical issues to design the broadband single-chip DTV tuner, such as harmonic mixing, image rejection, dynamic range, and linearity [1]. DTV broadcasting environments with multiple strong interferers degrade the selectivity and linearity performances of DTV tuner. Moreover, when wideband DTV tuners receive lower band channels, the harmonics of the local oscillator will occur in the same DTV band which is different from narrowband RF receivers. Therefore, the rejection of harmonics is important for DTV tuner design.

Figure 1 describes harmonic mixing problem in a low or zero IF receiver which has a wide input frequency range from 48 to 862 MHz. The switching operation of the mixer, result in harmonics of the local oscillator (LO) frequency. In the RF frequency range from 48 to 287 MHz, wanted signal and harmonics signal are down-converted to the desired signal band which results in the degradation of signal to noise ratio (SNR). Therefore, the harmonic rejection mixer (HRM) working from 48 to 287 MHz is required to solve harmonic mixing problem.

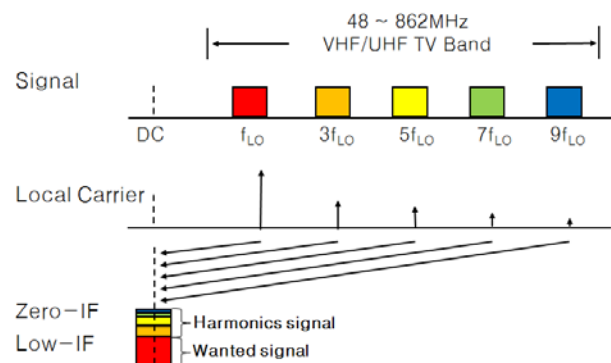


Figure 1. Harmonic mixing problem.

In previous research, harmonic mixing problem has been solved by using up-down dual conversion mixer [1, 2] or poly-phase mixer [3, 4]. However, up-down dual conversion mixer requires bulky off-chip SAW filter which cannot be fully integrated. A low power, small size and single chip silicon tuner is key element for digital TV. Therefore, for full integration, a poly-phase mixer topology is adopted in this paper to solve harmonic mixing problem. Conventional poly-phase HRM adopts Gilbert mixer architecture which can provide good RF and LO stage isolation [3, 4]. However, it requires high supply voltage for enough voltage headroom. Therefore, it is not suitable for design with scaling down CMOS technology under low supply voltage. Moreover, linearity is poor because of limited voltage headroom. In this paper, a novel low-power and high linearity HRM which adopts current-reused folded cascode type mixer is presented. Proposed HRM can achieve 41.1~41.5 dB 3rd-order harmonic rejection ratio in the frequency range from 48 to 287 MHz. Section II introduces the circuit design of proposed HRM. Section III shows simulation results of the circuit. Finally, conclusion is given in section IV.

II. CIRCUIT DESIGN

A. Harmonic Rejection Mechanism

Normally, switching stage of the mixer requires multi-phased LO signal for the harmonic rejection [5]. To eliminate third and fifth harmonics of the switching operation efficiently,

$\pi/4$ phase shifted LO signals are mostly used due to the simple circuitry.

Figure 2 shows the $\pi/4$ phase shifted LO signals (LO1(t), LO2(t), and LO3(t)) and summed signal (LO(t)) which is quantized by summation of scaled LO signals amplitude (1: $\sqrt{2}$:1). In order to show the harmonic rejection mechanism from these LO signals, the Fourier series of each square wave are given by

$$LO1(t) = \frac{2}{\pi} \left[\cos(\omega t + 45^\circ) - \frac{1}{3} \cos 3(\omega t + 45^\circ) + \frac{1}{5} \cos 5(\omega t + 45^\circ) - \frac{1}{7} \cos 7(\omega t + 45^\circ) \dots \right] \quad (1)$$

$$LO2(t) = \frac{2}{\pi} \left[\cos(\omega t) - \frac{1}{3} \cos(3\omega t) + \frac{1}{5} \cos(5\omega t) - \frac{1}{7} \cos(7\omega t) \dots \right] \quad (2)$$

$$LO3(t) = \frac{2}{\pi} \left[\cos(\omega t - 45^\circ) - \frac{1}{3} \cos 3(\omega t - 45^\circ) + \frac{1}{5} \cos 5(\omega t - 45^\circ) - \frac{1}{7} \cos 7(\omega t - 45^\circ) \dots \right] \quad (3)$$

$$LO(t) = LO1(t) + \sqrt{2} LO2(t) + LO3(t) = \frac{4\sqrt{2}}{\pi} \left[\cos(\omega t) - \frac{1}{7} \cos(7\omega t) \dots \right] \quad (4)$$

Equation (4) describes a summation of LO1(t), LO2(t) and LO3(t). Especially, the amplitude of the LO2(t) is scaled by $\sqrt{2}$ to obtain highest harmonic rejection [5]. As can be seen in (4), the third and fifth harmonics is removed and only ignorable high order harmonic is remained. Therefore, the harmonic mixing problem can be mitigated by driving the mixer switching stage with the quantized LO signals, as shown in Figure 2.

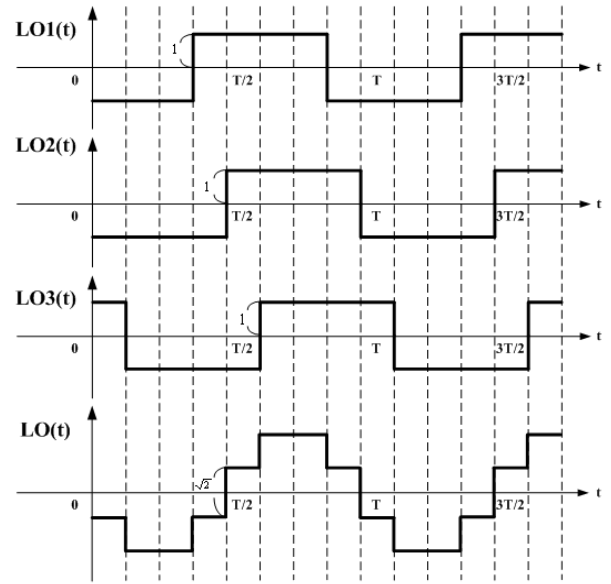


Figure 2. Quantized LO(t) signal generation.

B. Harmonic Rejection Mixer Design

Figure 3 shows the proposed current-reused folded cascode HRM. The proposed HRM constitutes with three transconductance stages (GM1, GM2, and GM3), three switching stages (SW1, SW2, and SW3), and one output load (R_L , C_L , M_{L1} , and M_{L2}). In the transconductance stage, current-reused technique is used to increase effective input transconductance and reduce the power consumption. In addition, source degeneration resistor (R_{deg}) is used to improve linearity. And resistive feedback (R_f) is used for self bias. The effective input transconductance of GM1, GM2, and GM3 is set to 1: $\sqrt{2}$:1 for the same ratio of LO signal amplitude as

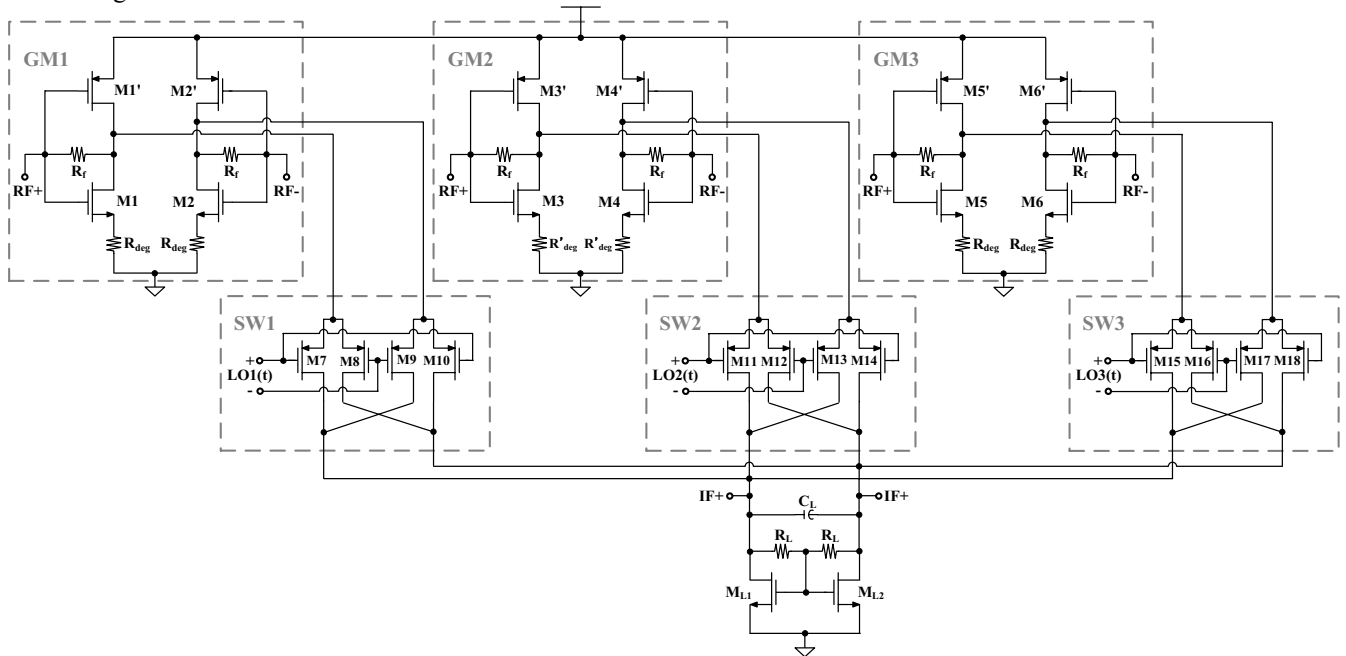


Figure 3. Proposed current-reused folded cascode harmonic rejection mixer.

mentioned before.

Each switching transistor pair (SW1, SW2, and SW3) operate independently by three LO signals, LO1(t), LO2(t), and LO3(t), and down converted IF signals are summed at the output node (IF+, IF-). In the output node, common-mode feedback circuitry (R_L , M_{L1} , and M_{L2}) is used to stabilize the DC operating point and reduce voltage drop at output load. And C_L is used for the suppression of the LO signals at the output node.

The proposed current-reused folded cascode HRM is suitable for low power and low supply voltage design in today's advanced CMOS technology. In addition, increased voltage headroom and source degeneration technique gives improved linearity performance.

III. SIMULATION RESULTS AND DISCUSSION

The proposed HRM is designed and simulated in the standard 0.13 μm CMOS technology. The proposed mixer operates in the frequency range from 48 to 862 MHz. Figure 4 shows 41.1~41.5 dB 3rd-order harmonic rejection ratio. For the high harmonic rejection ratio, accurate phase LO signals and exactly scaled transconductance ($\sqrt{2}$ times transconductance) are important factors. Since harmonic mixing problems are dominant only in the frequency range of 48~287 MHz, Figure 4 shows harmonic rejection ratio from 48 to 287 MHz. Figure 5 shows 6~9.9 dB voltage gain in the whole frequency range. Figure 6 and Figure 7 show the simulated NF and IIP3, respectively: 10.9~11.3 dB NF and 5.3~9.8 dBm IIP3 in the whole frequency range. Since LO signals are close to IF frequency (4MHz), it is difficult to fully suppress LO signals by output capacitor C_L . Therefore, NF performances are degraded in the low input frequency. And it is noticeable that the proposed mixer has good linearity performance even in the low power consumption which is very suitable for DVB-T tuner. The summarized performance of the HRM is shown in Table I.

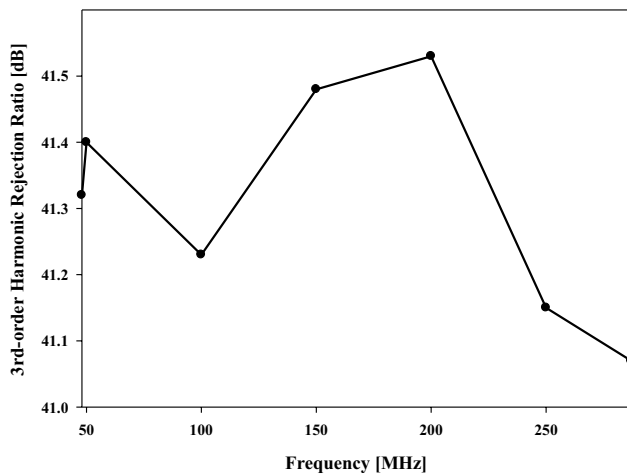


Figure 4. Simulated 3rd-order harmonic rejection ratio.

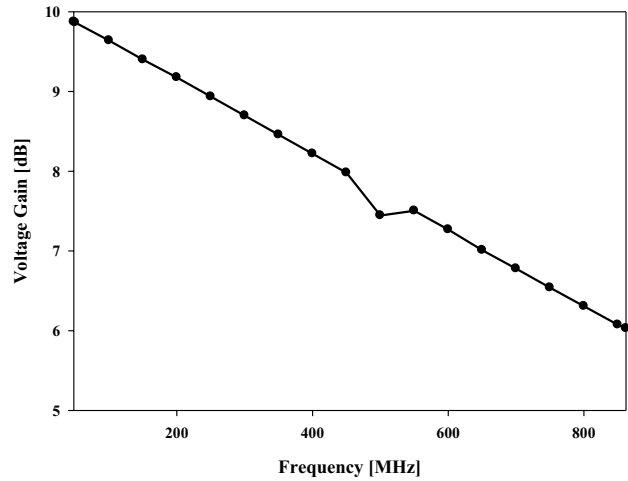


Figure 5. Simulated voltage gain.

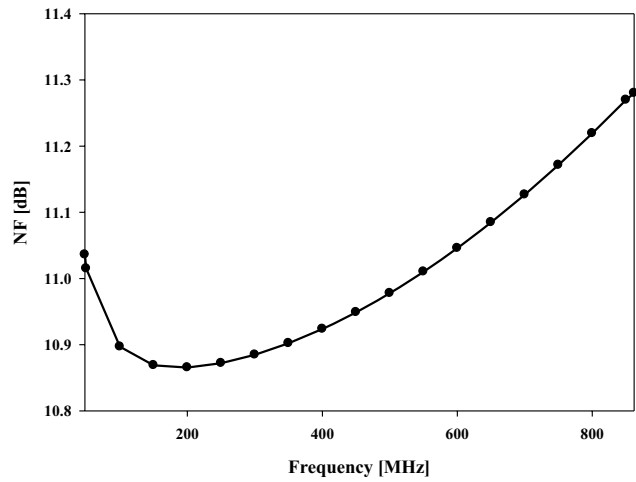


Figure 6. Simulated NF.

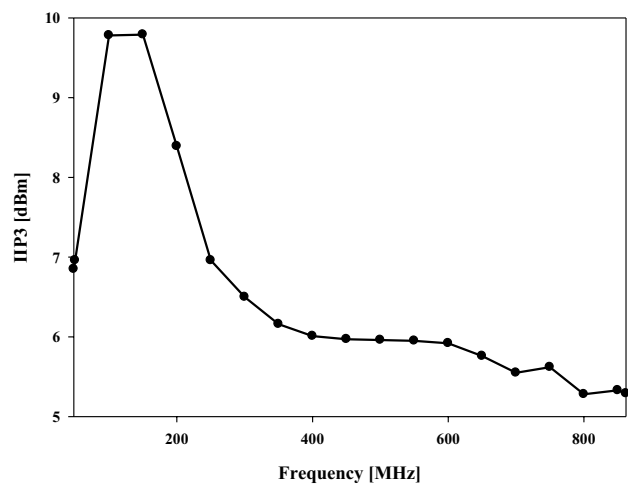


Figure 7. Simulated IIP3.

TABLE 1. PERFORMANCE SUMMARY OF HRM

Parameters	Results
Technology	0.13um CMOS
Supply voltage	1.2V
Current consumption	1.5mA
Operating frequency	48~862 MHz
3 rd -order harmonic rejection ratio (48~287MHz)	41.1~41.5 dB
Voltage gain (48~862MHz)	6~9.9 dB
NF (48~862MHz)	10.9~11.3 dB
IIP3 (48~862MHz)	5.3~9.8 dBm

IV. CONCLUSIONS

This paper presents a novel low-power current-reused folded cascode HRM for DVB-T application. It can solve the harmonic mixing problem in DTV tuner design. A low-power consumption and high linearity are achieved by using proposed current-reused folded cascode HRM. Simulation results show 41.1~41.5 dB 3rd-order harmonic rejection ratio in the frequency range of 48~287 MHz, 6~9.9 dB voltage gain, 10.9~11.3 dB NF, and 5.3~9.8 dBm IIP3 in the frequency range of 48~862MHz. These features are obtained consuming only 1.5mA current from a 1.2V supply in a standard 0.13um CMOS technology.

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REFERENCES

- [1] Mark Dawkins, Alison Payne Burdett, and Nick Cowley, "A Single-Chip Tuner for DVB-T", IEEE journal of solid-state circuits, vol.38, no. 8, August 2003.
- [2] Mehr, I.; Rose, S.; Nesterenko, S.; Paterson, D.; Schreier, R.; L'Bahy, H.; Kidambi, S.; Elliott, M.; Puckett, S.; "A dual-conversion tuner for multi-standard terrestrial and cable reception", VLSI Circuits, 2005, 16-18 June 2005 Page(s):340 – 343.
- [3] M. Gupta, S. Lervasteesin, D. Kang, and B-S. Song, "A 48-to-860MHz CMOS direct-conversion TV tuner," ISSCC 2007, pp. 206-207.
- [4] Maxim, A.; Johns, R.; Dupue, S.; "0.13u CMOS hybrid TV tuner using a calibrated image and harmonic rejection mixer," VLSI Circuits, 2007 IEEE Symposium on, 4-16 June 2007, pp. 206 – 207.
- [5] Weldon, J.A.; Narayanaswami, R.S.; Rudell, J.C.; Li Lin; Otsuka, M.; Dedieu, S.; Luns Tee; King-Chun Tsai; Cheol-Woong Lee; Gray, P.R.; "A 1.75-GHz highly integrated narrow-band CMOS transmitter withharmonic-rejection mixers", Solid-State Circuits, IEEE Journal of, vol. 36, Dec 2001, pp. 2003-2015.