

A CMOS Power Amplifier for UHF RFID Reader Systems

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Abstract— This paper presents a CMOS single-ended power amplifier for UHF RFID reader system-on-chip. Since the power amplifier for RFID reader demands high power gain and linearity, the designed power amplifier adopts two-stage structure which has a class-A operation. The power amplifier is designed and fabricated using commercial 0.13 μm CMOS process. Its chip size is 500X420 μm^2 . It is operated at a frequency range of 900 MHz with a supply voltage of 3.3 V. The measured output 1-dB compression point (P1dB) and power gain with a single-tone input are 17.7 dBm and 31.7 dB, respectively. A power-added efficiency (PAE) at P1dB is about 27 %. A 3rd-order intermodulation distortion (IMD3) of lower than -30 dBc is maintained up to 14.06 dBm for an output power. The maximum output 3rd-order intercept point (OIP3) was measured by 27.32 dBm at an output power of 11.27 dBm.

Keywords— CMOS power amplifier, single-ended power amplifier, radio frequency identification (RFID), UHF RFID reader.

I. INTRODUCTION

Advanced integrated circuit technology based on very cheap CMOS technology enables the radio frequency identification (RFID) to be more and more popular. RFID can be applied for various industries or organizations, such as toll road, parking area access, intermodal freight container identification, pallet tracking, railroad and truck (rolling stock) tracking, animal identification, work-in-progress tracking, matching passengers with their bags at airports, and so on [1], [2].

Especially, ultra high frequency (UHF) RFID systems have much longer reading range of 3 to 10 m, compared to the low frequency (LF) of either 125 or 134 kHz or high frequency (HF) of 13.56 MHz. Far-field tag operating at the UHF band has an advantage. That is a capability of the small antenna, which results in low fabrication and assembly costs for fast spread and adoption to various applications [3].

An RFID system consists of readers (also called interrogators) and tags (or transponders) [4]. Figure 1 is a simplified block diagram for the transmitter (Tx) part of the RFID reader. Output signal from the reconstruction filter is converted to UHF band by the up-conversion mixer. After up-conversion, the power amplifier delivers the modulated RF signal to the antenna [5]. Power amplifier block includes a driver power amplifier and an external power amplifier.

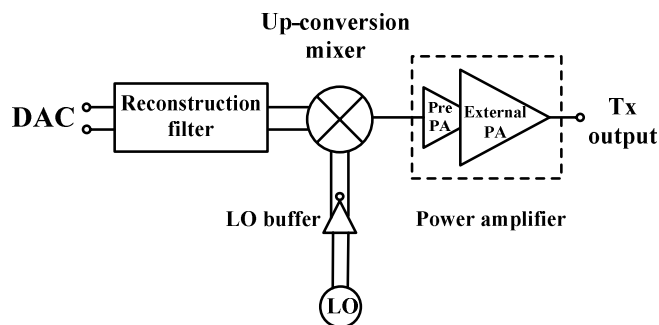


Figure 1. A simplified block diagram for the Tx part of the RFID reader

In this paper, a driver power amplifier is designed and implemented for RFID reader system-on-chip (SoC). The CMOS on-chip driver power amplifier is required to have a good linearity for the linearity of the overall power amplifier. It has a two-stage configuration and class-A operation for a sufficient gain and high linearity, respectively. It also has a single-ended structure for simpler circuit configuration than the balanced structure.

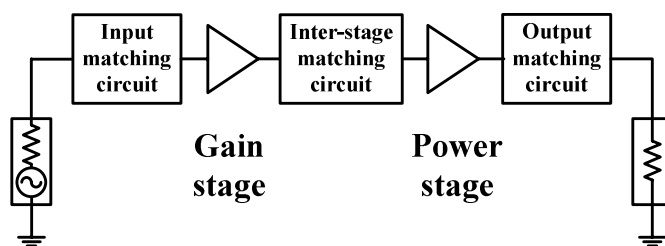


Figure 2. A simplified block diagram of the two-stage power amplifier.

II. CIRCUIT DESIGN

Figure 2 shows a simplified block diagram of the CMOS power amplifier which has a two-stage single-ended structure. A single-ended configuration avoids input and output baluns, thus making the power amplifier IC be smaller and cost-effective [6].

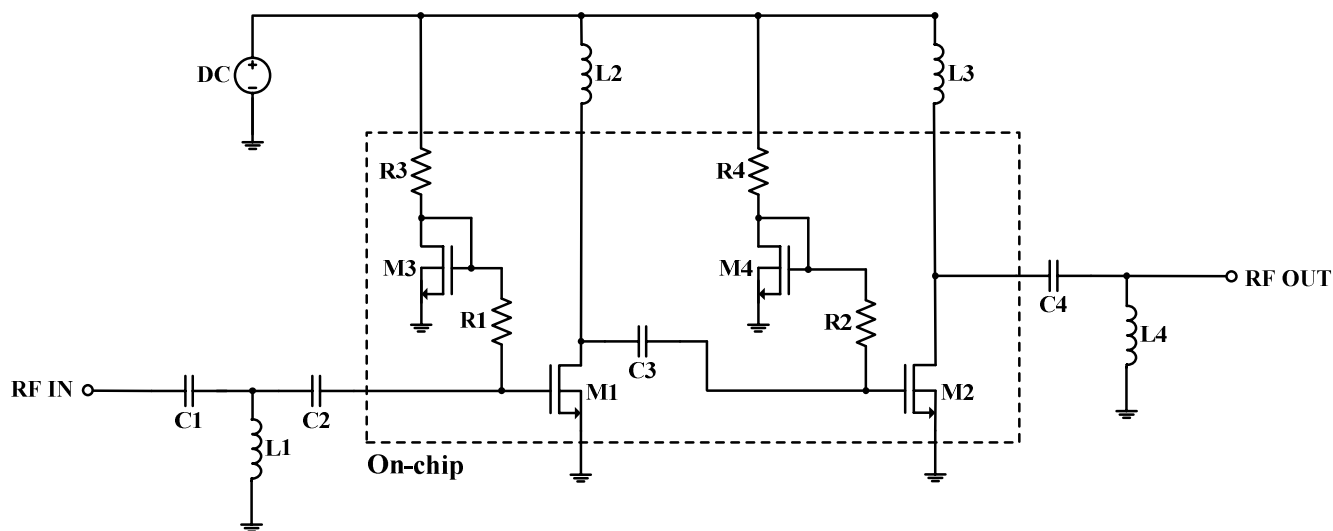


Figure 3. A detailed schematic diagram of the two-stage single-ended CMOS power amplifier.

The inter-stage matching circuit, including series on-chip capacitor and shunt off-chip inductor, is located between the gain stage and the power stage. The shunt inductor is also used to supply a drain bias. The input impedance matching circuit in front of gain stage is designed using a source pull method and the output impedance matching circuit after the power stage is designed using a load pull method.

Figure 3 is a detailed schematic diagram of the two-stage single-ended CMOS power amplifier. The components in the input matching and output matching networks, and the shunt inductor, L2, in the inter-stage matching network are implemented on off-chip in order to reduce the chip size. The value of the on-chip series capacitor, C3, in the inter-stage matching network was optimized as 3.6 pF between the size and performance.

The gain stage consists of the active DC bias circuit, transistor M1, and RF choke inductor, L2. The power stage also consists of the active DC bias circuit, transistor M2, and RF choke inductor, L3.

The active bias circuits of the power amplifier are composed of four resistors of R1, R2, R3, and R4, and two transistors of M3 and M4 for reference current generation. DC blockings are provided by capacitors C2 and C4. The active bias circuit is adopted to have better insensitivity on temperature and process variations.

Sizes of the power transistors are an important design issue to obtain an appropriate output power. In this CMOS power amplifier design, power transistor cells were designed by combining MOSFET to be a gate finger length of 0.35 μm . The total width of a unit transistor's gate is 50 μm .

Layout design can strongly influence on the performance of the power amplifier especially at high frequencies. In order not to lose its simulated performance, the effects of parasitic components, thermal distribution, and signal coupling should be carefully considered in the layout design.

The power amplifier IC is fabricated using 0.13 μm CMOS process and occupies an area of 500X420 μm^2 . To avoid a

electro-migration, the width of metals and type of metal layers are carefully chosen after considering the quantity of currents. The RF signal path is designed to be as short and straight as possible.

III. EXPERIMENTAL RESULTS

A CMOS power amplifier for the UHF RFID reader systems were fabricated using 0.13 μm CMOS process. Figure 4 shows the die microphotograph of the power amplifier IC. The overall circuit was evaluated on a printed circuit board which was implemented using FR-4 and whose size is as small as 33X39 mm^2 . The implemented CMOS power amplifier IC was evaluated using 900 MHz input signal with a single bias supply of 3.3 V.

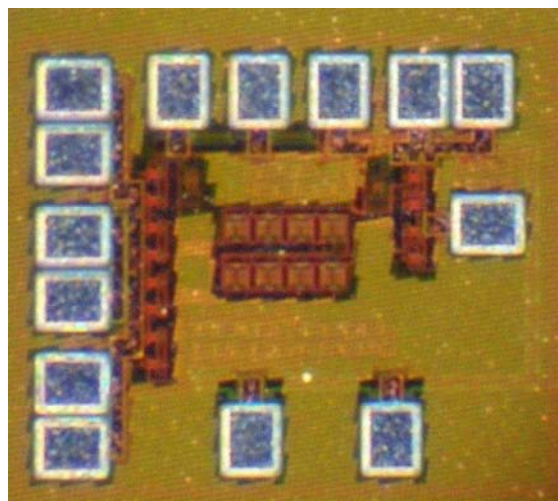


Figure 4. The die microphotograph of the fabricated power amplifier IC based on 0.13 μm CMOS process.

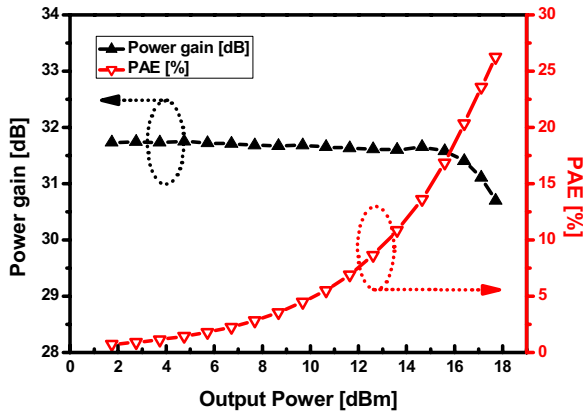
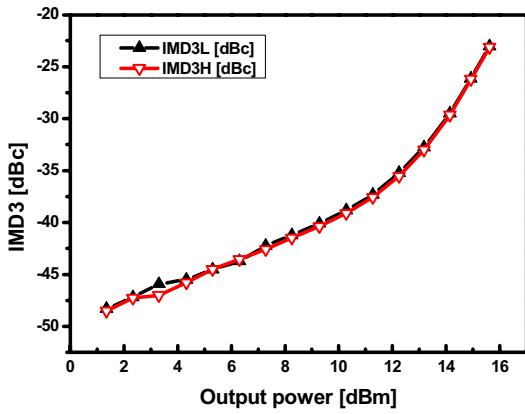
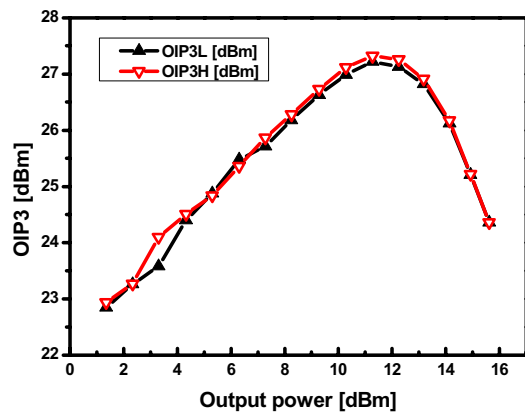


Figure 5. The measured power gain and PAE according to output power for the single-tone input.



(a)



(b)

Figure 6. The measured IMD3 (a) and OIP3 (b) according to output power for the two-tone input.

TABLE 1. MEASURED PERFORMANCES OF THE CMOS POWER AMPLIFIER IC

Parameter	Performance	
Vbias (V)	3.3	
DC current (mA)	Gain stage	19
	Power stage	43
Power gain (dB)	31.7	
P1dB (dBm)	17.7	
PAE (%)	27.0 @ P1dB	
IMD3 (dBc)	-30 @ output power 14.06 dBm	
OIP3 (dBm)	27.32 @ output power 11.27 dBm	

The experiment results are summarized in Table 1. The power gain, PAE, 1 dB compression point (P1dB), and output 1 dB intercept point (OIP3) were measured. Figure 5 shows the measured power gain and PAE according to output power for the single-tone input. The measured power gain is 31.7 dB and output 1dB gain-compression point (P1dB) is 17.7 dBm. The PAE is 27 % at P1dB.

To verify its linearity performance, power amplifier was tested using the two-tone signal with a center frequency of 900 MHz and a tone-spacing of 400 kHz. The third-order intermodulation distortion (IMD3) and OIP3 were obtained as -30 dBc at an output power of 14.06 dBm and 27.32 dBm at an output power of 11.27 dBm, respectively, as shown in Figure 6.

IV. CONCLUSIONS

In this paper, a single-ended two-stage CMOS power amplifier IC was designed and implemented for UHF RFID reader. The chip was fabricated using 0.13 μm CMOS process and occupies an area of 500X420 μm^2 . The implemented CMOS power amplifier IC delivered a high P1dB of 17.7 dBm with a power gain of 31.7 dB and a PAE of 27 % at P1dB. The IMD3 maintains below -30 dBc for an output power up to 14.06 dBm. The maximum OIP3 is 27.32 dBm at an output power of 11.27 dBm. The experimental results prove that the driver power amplifier IC, designed in this work, exhibited good performances enough to drive the external power amplifiers in the RFID readers.

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