

Modeling Router Hotspots on Network-On-Chip

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Abstract— A Network-on-Chip (NoC) is a new paradigm in complex System-on-Chip (SoC) designs that provides efficient on-chip communication architecture. It offers scalable communication to SoC and allows decoupling of communication and computation. In NoC, design space exploration is critical due to trade-offs among latency, area, and power consumption. Hence, analytical modeling is an important step for early NoC design. This paper presents a novel top-down approach router model, and utilizes this model for analysis mesh NoC performance measured in terms of throughput, average of queue size, efficiency, loss and waiting time. The model is used also to represent utilization of NoC infrastructure resources.

Keywords— Markov chain, Mesh, Modeling, Network-on-Chip (NoC), Queue, Quality-of-Service (QoS), Router Hotspots.

I. INTRODUCTION

Network-on-chip (NoC) has been proposed [1] to replace system bus as the primary on-chip communication method. Due to the separation of computation and communication, NoC could be designed separately from the computational entities (termed intellectual properties, IPs) [2]. Hence, analysis and optimization of NoC performance in terms of waiting time (delay), latency, and loss are required. Quality-of-Service (QoS) for NoC defines the level of commitment for packet delivery among IPs. Such a commitment can be the correctness and completion of the transaction, and bounds on the performance [3].

Researchers addressed the NoC router modeling from different perspectives [4] and [5]. The work in [5] proposed a delay model for a variable pipelined wormhole router with fixed time cycle to address Lopez's model problem. However, these models cannot be applied for router designs that use both clock edges and furthermore they did not study the impact of changing router design parameters on its delay. The router queue modeling also still need to be addressed because it is very important to get an estimation of the optimum queue size that matches the target traffic characteristics at higher levels of abstraction.

Different NoC-based SoC applications require different NoC design aspects in terms of the topology, router type, queue size, and switching technique. The challenges for NoC research have thus been on assisting early design space exploration for NoC-based SoC. Good traffic and NoC performance estimation could significantly shed some light to

probable NoC design aspects. This work looks at router model that estimates an NoC router performance. This paper presents a performance analysis of mesh NoC in terms of throughput, average queue size, efficiency, loss, and waiting time. A discrete time Markov model of mesh NoC topology is obtained, which helps decision-making in terms of switching techniques, buffer sizes, and router types. This also helps to identify router and link hotspots for better packet routing.

The rest of the paper is organized as follows. In Section II, we discuss related works on modeling NoC infrastructure. Section III presents the NoC structure issues. Section IV proposes the Markov chain modeling of NoC. Finally, Section V concludes this paper.

II. RELATED WORKS

System bus is a circuit-switching, connection-oriented on chip communication backbone. In contrast, NoC uses packet switching, which segments the message into a sequence of packets [6] sent to a shared network. On-chip networks share the same characteristics in topology, switching, routing, and flow control with local area network [7]. Furthermore, NoC has to provide high and predictable performance [8] with small area overhead and low power consumption.

An important problem in NoC is the router design, because it significantly affects the network performance and power consumption. An efficient router design is determined by its switching technique (packet switching, wormhole, etc.), flow control type (hand shaking, credit based, etc.), queue size, arbiter design (round robin, rate-proportional servers, etc.) and routing scheme (adaptive, deterministic). Researchers tried to address the design and modeling of NoC routers from different perspectives. In this subsection, we highlight the work done up to date in this area through representative research work.

Chien et al. [9] proposed a delay model for wormhole and virtual channel routers. However, this model was designed for 0.8-micron CMOS and also cannot be applied to pipelined architectures. The router queue modeling also still need to be addressed because it is very important to get an estimation of the optimum queue size that matches the target traffic characteristics at higher levels of abstraction. Due to limited buffers [10] and link bandwidth, packets may be blocked due to contention [11]. Buffer sizing has a direct association with bounds in bandwidth, delay and jitter [12].

III. NOC STRUCTURE

This section provides background on NoC architectural issues. These issues include network topology, router structure, switching techniques and routing algorithms. The trade-off analysis in NoC modeling can be performed by optimally considering NoC architecture parameters based on a specified application.

A. Topology

This architecture is based on an $m \times n$ mesh network where every router, except those at the edges, is connected to four neighbouring routers and one computation resource, (IP) through communication channels [13]. This topology allows integration of large number of IP cores in a regular shape structure. A channel consists of two unidirectional links between two routers or between a router and a resource. Fig. 1 shows a 3×3 mesh NoC with nine functional IP blocks.

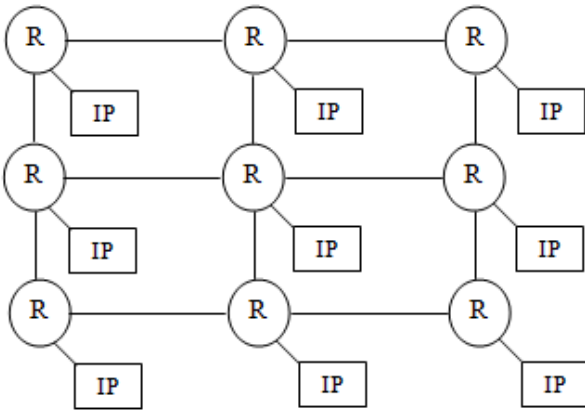


Figure 1. Mesh Topology

B. Router Structure

Router operates at the network layer similar to the one for computer network. A router uses packet headers and a forwarding table to determine the best way a packet should go between the networks. An NoC router has three main architectural components, which are input/output ports, queues, and Switch Fabric (SF). The switch fabric establishes the required paths between pairs of input and output ports according to a certain routing mechanism such as round-robin scheduler, weighted round-robin scheduler, and max-min fairness scheduling [14]. Fig. 2 shows an input-queuing router. Each input port has a dedicated First-In-First-out (FIFO) queue for storing incoming packets. In one time step, an input queue must be able to support one write and one read operations. Assuming an $n \times n$ router, the switch fabric must connect n input ports to n output ports [14].

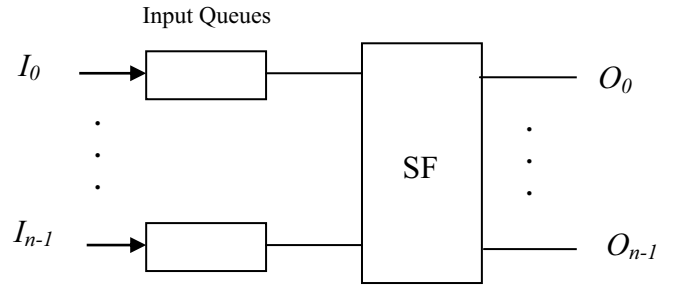


Figure 2. Input-queuing router

C. Routing

Routing algorithms are used to specify the path from source to destination for each message. They can be implemented in two ways which are either deterministic or adaptive [15]. Deterministic routing protocol chooses the path for a message only by its source and destination. All packets with the same source and destination pair will follow one single path. The packet will be delayed if any channel along this path is loaded with heavy traffic, and if a channel along this path is faulty, the packet cannot be delivered. Thus, the deterministic routing protocols suffer from poor use of bandwidth and blocking even when alternative paths are available. This work assumes deterministic routing, where packets with the same source and destination always traverse the same path [15].

IV. MARKOV CHAIN APPROACH FOR NETWORK-ON-CHIP MODELING

There are several approaches to modeling NoC. Several works [1]–[3] and [6] focus on stochastic models. This project could be conceptualized from top-level system design. It starts with the highest level of NoC view, and works its way down to every single component in NoC block diagram.

A. Modeling Abstractions

An NoC-based SoC system is composed from an NoC topology and IP blocks. The NoC provides decoupling computation (IP) and communication parts. This allows for IPs and interconnects to be designed independently. At a level below is the router abstraction. Routers are pivotal modules in NoC based design.

1) *NoC-level Abstraction*: Fig. 3 shows a SoC system is composed from NoC and IP blocks. The NoC provides decoupling computation (IP) and communication parts. This allows for IPs and interconnects to be designed independently.

2) *Topology-level Abstraction*: Fig. 1 shows the top level view of a 3 mesh topology for NoC modeling. Two elements on NoC are router and network interface (NI). The NI is used as interfaces between IP blocks and NoC. Function of the router is to transport data from one network interface to another. This work considered analysis on NoC router only.

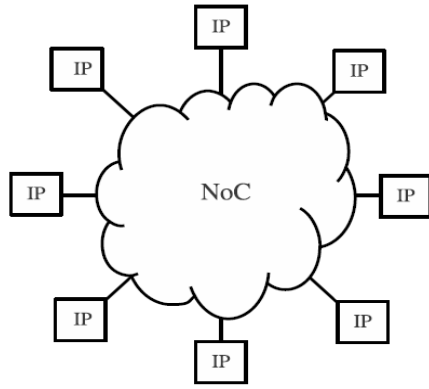


Figure 3. NoC-level Model Abstraction

3) *Router-level Abstraction*: Mesh topology is used with each router has the maximum 5 input-output ports. Four ports are connected with others routers and one port to the IP. Fig. 2 shows an input-queuing router internal structure. Each input port has a First-In-First-Out (FIFO) queue for storing incoming packets. In mesh topology, the top queue is fed by the link connected to the IP associated with that router and the other four bottom queues are fed by the inter-router links.

B. Performance Metrics

The NoC performance is analysed in terms of throughput, average queue size, and packet delay.

- 1) Throughput in units of packets per time step which demonstrate how many end-to-end packet/flit transfers.
- 2) Waiting time in terms of time step, where time step is defines as the time to transfer a packet on a local link (between two routers or between an NI and a router).
- 3) Average lost traffic is measured in units of packets per time step.
- 4) Queue Occupancy Queue size is measured in units of packets.

C. Queue Modeling

This section presents an analytical model for input-queuing router. Each queue is considered as a First-In-First-Out (FIFO) queue. The model has simple close-form calculations and produces the performance of the queue.

A simple $M/M/1/B$ queue is used in this model. This model provides a discrete-time Markov chain [14] analysis of queue where the time step is taken equal to the time required to transmit a packet. Poisson distribution traffic arrival process and the exponential distributed service time are assumed. For each queue model, one server queue with B finite buffer size is assumed.

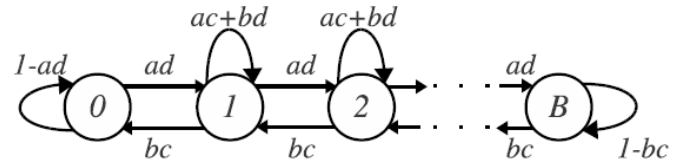


Figure 4. State transition diagram for an $M/M/1/B$ queue

Fig. 4 shows, the state transition diagram for the discrete time Markov chain $M/M/1/B$ queue. A homogeneous Markov Chain is considered since packet arrivals and departures are independent of the time index value [14]. With an assumption that a packet cannot arrive and be served in the same time slot. Each state represents the number of e-mails in the queue. In Fig. 4, $b = (1 - a)$ and $d = (1 - c)$ where:

- a : Probability of packet arrival
- b : Probability that a packet not arrive
- c : Probability that a packet leaves the queue
- d : Probability that a packet does not leaves the queue.

From state transition diagram in Fig. 4, the state transition matrix $\mathbf{P}$ [14] is defined as:

$$\mathbf{P} = \begin{bmatrix} 1-a & bc & \cdots & 0 & 0 \\ a & f & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & f & bc \\ 0 & 0 & \cdots & ad & 1-bc \end{bmatrix} \quad (1)$$

The difference equations for the state probability vector [14] can be expressed as:

$$\mathbf{s} = [s_0 \ s_1 \ \dots \ s_{B-1} \ s_B]^t \quad (2)$$

where s_i is the probability that the queue contain i packets, and is given as:

$$s_i = \rho^i d^{i-1} s_0 \quad \text{for } 1 \leq i \leq B \quad (3)$$

with ρ is defined as

$$\rho = \frac{a}{bc} \quad (4)$$

Satisfying the condition $\sum_{i=0}^B s_i = 1$ from [14] gives:

$$s_i = \frac{(1-\rho d)\rho^i d^{\max(0,i-1)}}{1+\rho(c-\rho^B d^B)} \quad \text{for } 0 \leq i \leq B \quad (5)$$

From Little's result [14], the average queuing waiting time, W is given by:

$$W = \frac{Qa}{Th} \quad (6)$$

where Qa is the average queue occupancy and Th is the average queue throughput. The throughput, Th , is defined as the probability that the queue is served while it is not empty, and is given by:

$$Th = c(1 - s_0) \quad (7)$$

The average queue occupancy Qa is given by:

$$Qa = \sum_{i=0}^B i s_i = \frac{1 - \rho d}{1 + \rho(c - \rho^B d^B)} \sum_{i=1}^B i \rho^i d^{i-1} \quad (8)$$

A packet is said to be lost when the queue is full when the packet arrives and none (in the queue) is serviced. Thus, the loss probability, L , is given by:

$$L = s_B ad \quad (9)$$

The queue size, B , gives a trade-off between queuing delay and loss probability. Bigger B increases the average queuing waiting time, W due to higher Qa and at the same time decreases the loss probability, and vice versa.

D. Router and NoC Modeling

This section discusses the placement of a router in mesh NoC can generate different value of output traffic c at each that router output port. It is also shows generation of general router performance. Router loading performance for each router is identified that determinates possible router hotspots in the NoC topology.

The output traffic of a router is an important value that significantly impact router performance in the network. Congestion condition occurs as soon as input traffic exceeds the maximum output traffic c as shown in Fig. 5. The congestion is characterized by decreased efficiency, increased packet loss and increased waiting time. Assuming that packet arriving at a certain input switching fabric router is destined to other $n - 1$ router output with equal probability c that depends on n . The general equation of output traffic c is:

$$c = \frac{\sum_{m=0}^{n-1} \frac{n!}{n-m}}{n \times n!} \quad \text{where } \frac{1}{n} \leq c \leq 1 \quad (10)$$

General router equation performance is generated from average of all queues in a router. There are the equations of throughput, efficiency, average queue size, loss and waiting time for a router r_i . The overall performance in terms of throughput, efficiency, average queue size, waiting time and loss are obtained by averaging all 16 routers in a 4x4 mesh NoC. The general NoC performance is given in Table I.

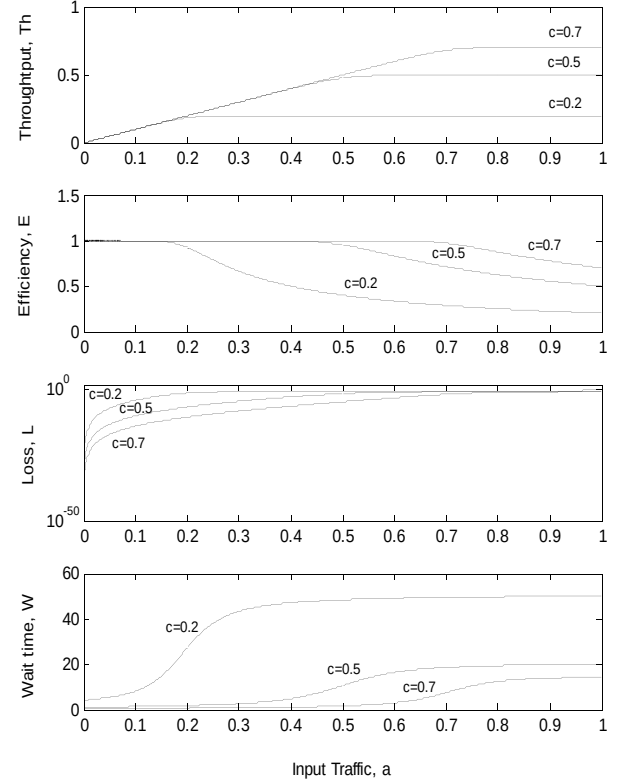


Figure 5. Performance of an $M/M/1/B$ queue. Throughput, efficiency, loss and waiting time versus input traffic.

TABLE I.
GENERAL ROUTER AND NoC PERFORMANCE EQUATIONS. q_j REFER TO j -Th QUEUE IN ROUTER r_i .

Variables	Router r_i	NoC
Throughput, Th	$\frac{1}{ N } \sum_{j=1}^N Th_{q_j}$	$\frac{1}{ r_{total} } \sum_{i=1}^N Th_{r_i}$
Queue occupancy, Qa	$\frac{1}{ N } \sum_{j=1}^N Qa_{q_j}$	$\frac{1}{ r_{total} } \sum_{i=1}^N Qa_{r_i}$
Loss probability, L	$\frac{1}{ N } \sum_{j=1}^N L_{q_j}$	$\frac{1}{ r_{total} } \sum_{i=1}^N L_{r_i}$
Waiting time, W	$\frac{1}{ N } \sum_{j=1}^N W_{q_j}$	$\frac{1}{ r_{total} } \sum_{i=1}^N W_{r_i}$

V. CONCLUSIONS

This paper presented a Markov chain model for identifying router loading and hotspots. NoC performance metrics such as throughput, waiting time, queue size, efficiency, and loss could be easily identified from the model output. As with most other research works, the models described in this work cannot yet be claimed that they are finished. There are many interesting possibilities for future research here and the most important of these are, extending this modeling approach with other NoC topologies, router types, and queue models.

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