

Efficient High-Speed Optoelectronic Interconnects Parameter Extraction Based on 3D Field Simulation

Ikechi Augustine Ukaegbu*, Tae-Woo Lee*, and Hyo-Hoon Park*

*Department of Electrical Engineering, Korea Advanced Institute of Science & Technology (KAIST),

119 Munjiro, Yuseong-Gu, Daejeon, 305-732, Korea

aus20@kaist.ac.kr

Abstract— As the speed of integrated circuits increases, inductive coupling becomes an issue for the packaging interconnect technologies. This paper describes equivalent circuit extraction based on 3D full wave simulation for optoelectronic transmitter packaging interconnects. Simulation and extraction are performed for two kinds of transmitter modules: planar and multi-chip modules. The extracted equivalent circuit model of the optoelectronic interconnects is accurate and can be applied in packaging design state-of-the-art.

Keywords— *Optical interconnection, multichip module, planar module, crosstalk.*

I. INTRODUCTION

Optical interconnection technology is one of the preferred and potential technologies for meeting with the high speed and bandwidth requirements of the next generation computer systems. Most optical components used in optical interconnection technology require electrical interconnects for power and signal transmission, and these electrical interconnects affect the performance and the overall bandwidth of the optical link. And as clock frequency reaches the gigahertz band with signal transmission rate reaching the gigabit range, signal integrity issues such as crosstalk between signals become serious issues in signal interconnects [1]. Thus, there is a growing interest in the inductance associated with these signal interconnects. Studies on hybrid flip-chip bonded optoelectronic technology have shown many advantages when compared to conventional wire-bonded optoelectronic packaging due to the reduction of electrical parasitics [2]. Two transmitter modules employing the two packing technologies have been designed and prepared for crosstalk analysis. The modules are a planar module and a multi-chip (MCM) module. The planar module uses the conventional wire-bonding for interconnect between the driver chip and the VCSEL while the MCM module employs the flip-chip bonding technology.

In this paper, we describe equivalent circuit extraction based on 3D full wave simulation for optoelectronic transmitter packaging interconnects. The equivalent circuit extraction was performed for two kinds of transmitter module packaging models: planar module and MCM module; and the electrical interconnects under study are those between the driver chip and the VCSEL chip of the transmitter modules. Crosstalk performance is evaluated for both modules to show the improvement of the multichip module over the planar module for optoelectronic interconnects.

II. DESIGN OF THE TRANSMITTER MODULES

The transmitter modules constitute of a driver IC and a VCSEL. The driver IC is fabricated in a 0.18 μm CMOS technology and operates at 5 Gb/s per channel. It has a dimension of 1.1mm x 1.2 mm x 0.52 mm and is made up of an input stage for compatibility with external circuits, a gain

stage for sufficiently amplifying input signals and a drive stage for driving the VCSEL [3]. The VCSELs used in this study are 850 nm 1x4 VCSEL array with a pitch of 250 μm between each channel and a dimension of 1mm x 0.45mm x 0.1mm. They operate up to 2.5 Gb/s per channel.

Teflon based evaluation board is used for the implementation of the transmitter modules. The planar transmitter module is prepared by attaching the driver IC and the VCSEL (top-emitting) array chip separately to the Teflon-based evaluation board with a conductive epoxy and then using wire-bonding (gold wires) technology to make the electrical connection between the two chips and between the driver IC and the Teflon evaluation board. The multichip module (MCM) is prepared using the flip-chip bonding process to contact on the top side of the bottom-emitting VCSELs. The module is then attached to the Teflon-based evaluation board. Figure 1 shows the planar and MCM transmitter modules and the interconnects under study.

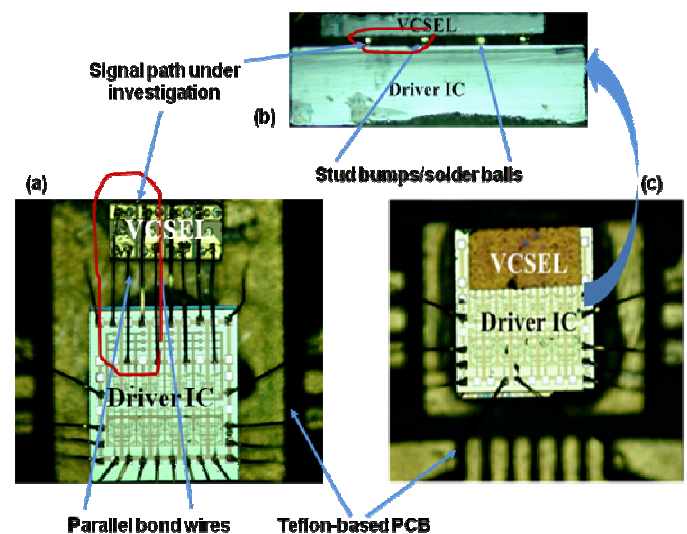


Figure 1. (a) The planar and (b), (c) MCM transmitter modules showing signal path (channels) under study

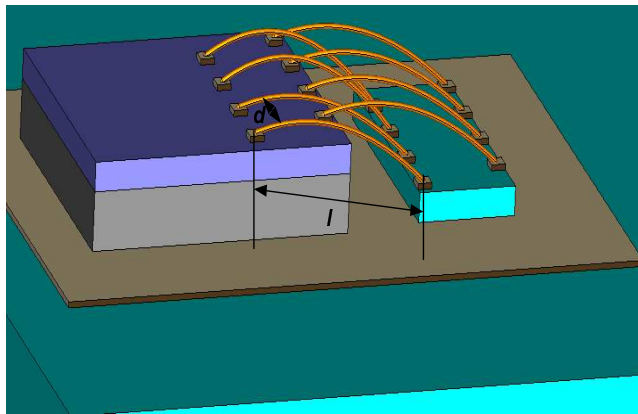
III. MODELLING AND FULL WAVE SIMULATIONS

Bond wires and stud bumps/solder balls are used for interconnects between components and chips. A decrease between these electrical interconnects implies an increase of coupling (crosstalk) and an increase in interference between the lines. In this section, we design the optoelectronic modules for full wave simulation and for equivalent circuit extraction. The signal paths under study are two parallel differential wirebond pairs (for the planar module) and two differential stud bumps/solder ball interconnect pairs (for the MCM module). Crosstalk is also investigated for weak coupling

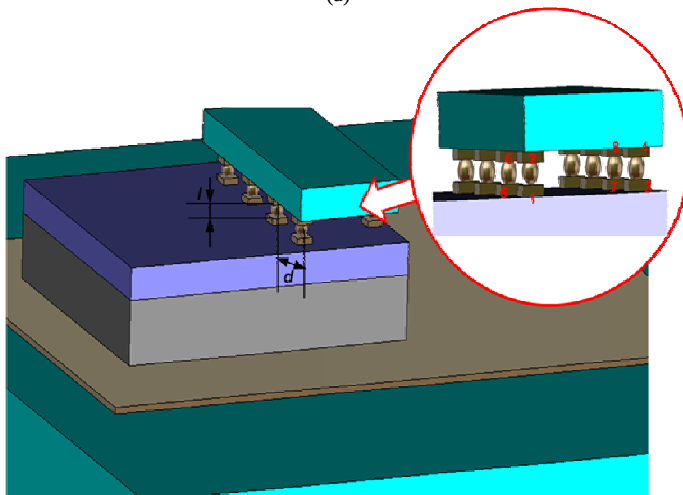
between the parallel pairs. This is the case where we consider the effect of differential pair one over the second differential pair and not vice versa [4], [5]. The wires are homogenous and have the same material properties for each of the modules. Excitation occurs during the operation of the transmitter module. At any particular time during the operation of the transmitter, the current in the aggressor line/pair induces current in the other line (victim line/pair) due to the mutual inductance and capacitance of the wires.

A. The IC model

The model consists of a silicon based driver IC and VCSEL chip packaged on the Teflon based evaluation board. The interconnect bondwires and solder balls for the electrical interconnect of the planar and MCM module were carefully designed, respectively with their bond pads. Figure 2 (a) and Figure 2 (b) show the modelled optoelectronic modules, where d represents interconnect separation distance, and l is interconnect length. The value of d is 250 μm for both modules while l is 60 μm for the MCM module and 700 μm for the planar module. Field simulation is performed with the simulation tool CST MicroWave Studio 3.0 (MWS).



(a)



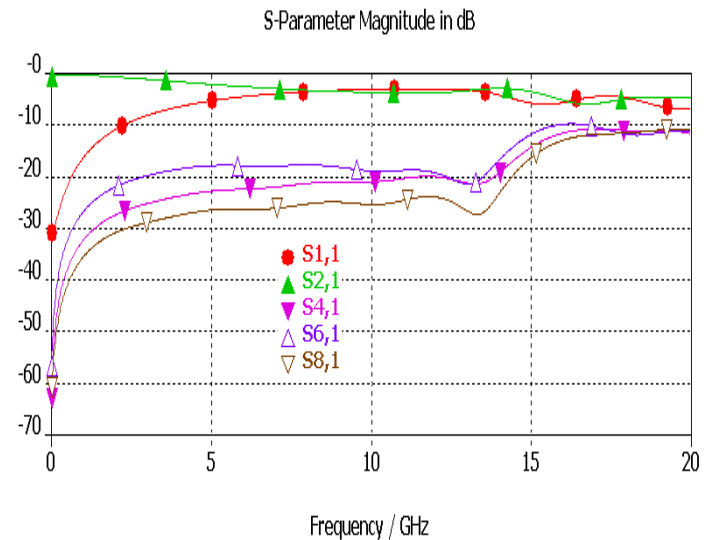
(b)

Figure 2. Packaged (a) planar and (b) MCM transmitter modules

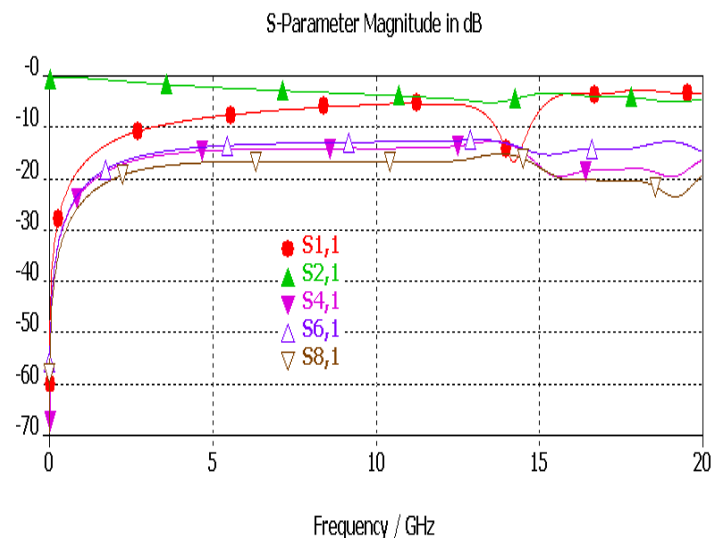
B. Field Simulation and Circuit Parameter Extraction

Several conventional circuit parameter extraction algorithms are based on static simulations of both the electric and magnetic field of the device to obtain equivalent values for the inductance and capacitance. And this approach does

not contain any dynamic behaviour of the circuit and thus the validity is limited to relatively low frequencies [6]. Our approach in this paper is based on RLC line model. It also considers each of the four interconnect lines as a transmission line. The transmitter modules are modelled in CST MW studio to investigate the crosstalk of the two modules. Eight discrete ports were used for the 3D simulation. The S-parameters obtained by time domain simulation in CST MWS are exported to ADS where the equivalent circuit parameters are computed. The operating frequency of interest is 0 to 20 GHz since we are considering high speed operation. All the metallic parts of the designed structure are assumed to be perfect electric conductive (PEC) and the other materials are defined by their conductivity and permittivity. Figure 3 (a) and Figure 3 (b) show the frequency response of the planar and MCM modules, respectively.



(a)



(b)

Figure 3. Full wave frequency response of the (a) planar module and (b) MCM module.

From the full wave simulations in Figure 3 (a) and Figure 3 (b), the MCM module experiences a higher crosstalk when compared to that of the planar module. This can be explained

as a result of increase in coupling capacitance between the driver chip and the VCSEL chip (between the input and output simulation ports) of the MCM module since the full wave simulation takes into consideration the effects of components within the neighbourhood of the interconnects. This is in addition to the parasitics being considered in the simulation. Also the simulation structures are different, with the MCM module consisting of stacked chips and the planar module with parallel chips. The multi-chip technology process involves the stacking of chips, one on top of the other. Thus, there is increase in capacitance between the two stacked chips and between the port pads. The planar module has the two chips parallel to each other on the same plane and therefore this parasitic capacitance is very much reduced. A control simulation was performed to verify the full wave simulation behaviour of the multi-chip module. This was done by designing a multi-chip module with an interconnect length similar to bondwire length. A higher crosstalk response was observed with the longer length MCM module when compared to the solder balls MCM. This therefore verifies crosstalk improvement when shorter interconnect lengths are used.

Figure 4 shows the expanded equivalent circuit model of two differential pairs. $L_1...L_4$, $C_1...C_4$, and $R_1...R_4$ represent inductance, capacitance, and resistance of each line, respectively. Mutual inductance and coupling capacitance are taken into consideration. C_1 and C_2 are the coupling capacitances in each pair while $C_{m1,eq}$ and $C_{m2,eq}$ model the coupling capacitance between the two pairs and the coupling capacitance between each pair and ground, respectively. Mutual inductance between the two parallel pairs is represented with $L_{m,eq}$ while L_{m1} and L_{m2} model mutual inductances within each pair. Figure 5 (a) and Figure 5 (b) show the compared frequency response of the packaging interconnects for the planar and MCM modules, respectively with circuit simulated parameters.

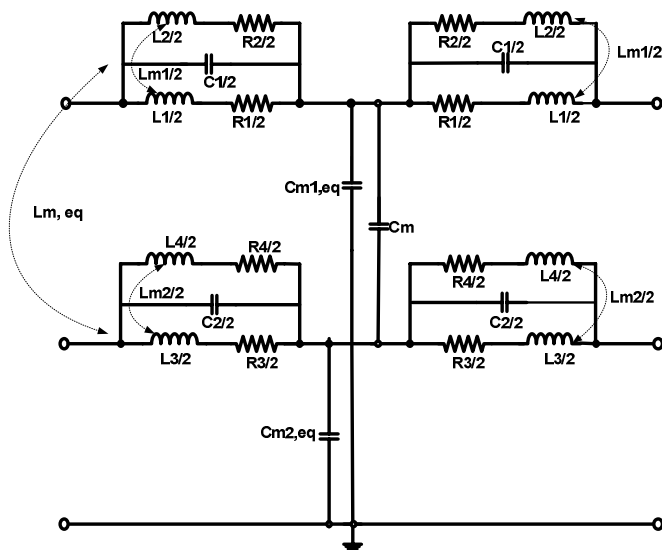
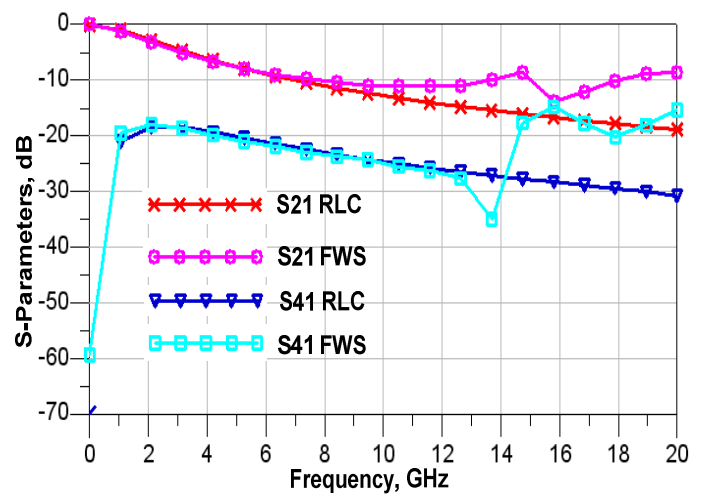
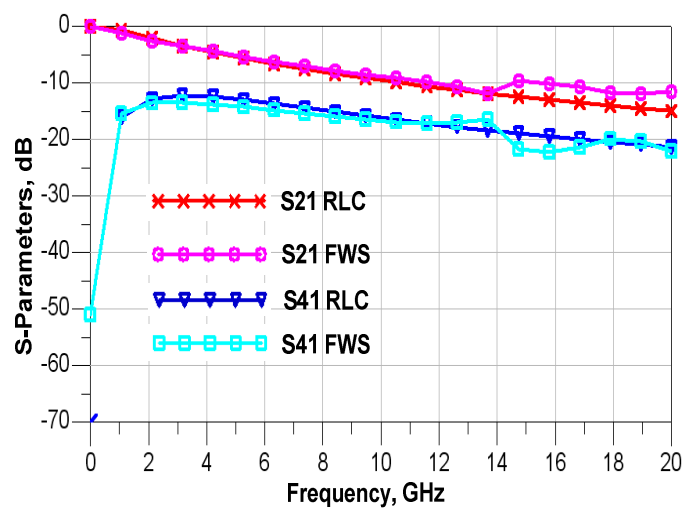


Figure 4. Extracted equivalent circuit model of the parallel pairs



(a)



(b)

Figure 5. Comparing the crosstalk of field and equivalent circuit model for (a) the planar module and (b) MCM module

There is good agreement between the extracted and field simulation model. This is because the extracted equivalent circuit model yields a good approximation of the parasitic behaviour of interconnects.

IV. CONCLUSIONS

In this paper, equivalent circuit extraction based on 3D full wave simulation of optoelectronic transmitter packaging interconnects has been described. The equivalent circuit extraction was performed for two kinds of transmitter module packaging models: planar module and MCM module. The equivalent circuit model is proposed for differential interconnect pairs between the driver chip and the VCSEL chip of the transmitter modules and is based on RLC line model. Crosstalk performance was evaluated for both modules to show the improvement of the multi-chip module over the planar module.

ACKNOWLEDGMENT

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