

Implementation of DSRC Mobile MAC for VANET

Sang-woo Chang, Jin-soo Jung, Jin Cha, Sang-sun Lee*

*Department of Electronics communication Computer Engineering Hanyang University
inthewood78@naver.com, jshomegenius@naver.com, chajjin2@naver.com, ssnlee@hanyang.ac.kr

Abstract—In this thesis, a Dedicated Short Range Communication(DSRC) Mobile Medium Access Control(MAC) algorithm to provide Vehicle-to-Vehicle(V2V) communication is implemented. Since the DSRC is a master-slave communication system, an On-board Equipment(OBE) does not have a function to transmit the Frame Control Message Channel(FCMC). To provide V2V communications, this thesis suggests an additional function for the FCMC transmission to a DSRC Mobile MAC(M-MAC) algorithm. The DSRC M-MAC algorithm for V2V is implemented through the Verilog-Hardware Description Language(HDL). The operational characteristics of the DSRC M-MAC algorithm supporting both V2I and V2V communications were tested. The tested operational characteristics are reception of Activation channel(ACTC) between a commercial Road-Side Equipment(RSE) and the developed OBE, transfer of ACTC between the developed OBE and a commercial OBE, transfer and reception of V2V message data between the developed OBEs.

Keywords— ITS, DSRC, VANET, V2V, MAC, FPGA

I. INTRODUCTION

Dedicated Short Range Communication(DSRC) that is one of the communication technologies for ITS, provides wireless link between Road-Side Equipment(RSE) and Onboard Equipment(OBE) in the range of 10m - 100m. DSRC infrastructure also has the installation expense problem to extend service zones. Vehicle-to-Vehicle(V2V) communication is good solution to extend the capability of the extant DSRC system. V2V communications can improve the qualities for both the road security service and the transportation management service.

TABLE 1. SPECIFICATION OF DSRC PHYSICAL LAYER

Items	Characteristics
Frequency Bandwidth	5.8GHz
Channel Bandwidth	10MHz
Data Rate	1Mbps
Transmission Distance	10 - 100m
Allowed Maximum Vehicle Speed	160Km/h
Modulation Type	ASK
Data Encoding Type	Manchester Coding
Bit Error Rate(BER)	$\sim 10^{-5}$

In this thesis, a V2V DSRC OBE Medium Access Control(MAC) algorithm is implemented. To provide V2V

communications, an additional function for the Frame Control Message Channel(FCMC) transmission to a DSRC Mobile MAC(M-MAC) algorithm is suggested. The DSRC M-MAC algorithm for V2V is implemented through the Verilog-Hardware Description Language(HDL). The operational characteristics of the DSRC M-MAC algorithm supporting both V2I and V2V communications were tested.

II. IMPLEMENTATION OF DSRC MOBILE MAC

In this chapter, the V2V DSRC M-MAC algorithm which is suggested in this paper is described.

A. Procedure of DSRC M-MAC

The procedure of DSRC OBE MAC algorithm applying the DSRC standard[1] is shown on the Figure 1.

1) When the FCMC is received, the Slot Control Identifier(SCI) fields in the FCMC are analysed. 2) It could have 3 types of state - transmission of Activation Channel(ACTC), receipt of Message Data Channel(MDC), and transmission of MDC. 3) If OBE MAC would like to initially access to the RSE, sending ACTC to the RSE. 4) Other cases are the receipt of or the transmission of MDC.

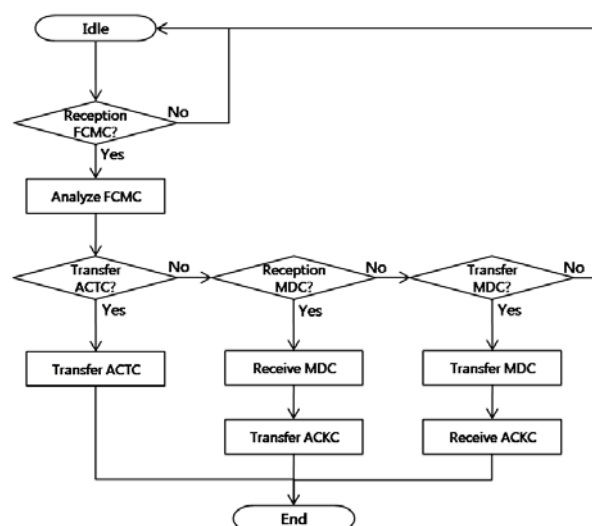


Figure 1. Procedure of DSRC OBE MAC

The procedure for V2V DSRC M-MAC algorithm modified in this paper is shown on the Figure 2.

1) To transmit the V2V message, the MAC prepares the FCMC and the MDC. 2) To prevent a collision, the MAC should confirm the presence of receiving data from Rx-side of DSRC modem. If it is idle, the MAC transmits the FCMC and the MDC to the OBEs in the communication area. 3) If it is busy, the MAC may defer the transmission and verify whether the receiving data is the FCMC. 4) If the receiving data is the FCMC, the MAC operates the V2I or V2V mode. 5) If the receiving data is not the FCMC, the MAC confirms the presence of receiving data again from Rx-side of DSRC modem and then it may try to transmit the V2V message.

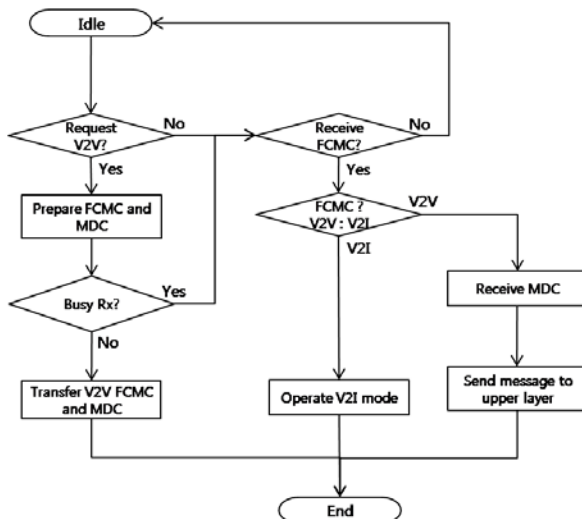


Figure 2. Procedure of DSRC Mobile MAC for V2V

B. Modification of MAC frame formats

To support the operation of the DSRC M-MAC for V2V, a few fields in the Frame Control Message Slot(FCMS) frame are re-defined modifying only the reserved fields. DSRC frame slots operating as the slotted ALOHA and FCMS frame format are shown on the Figure 3.

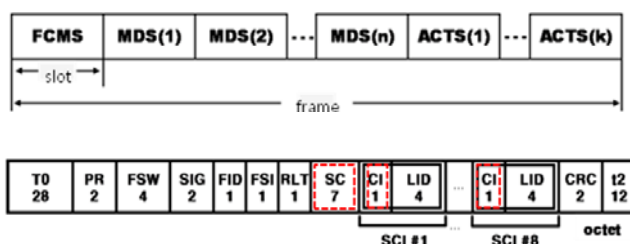


Figure 3. DSRC frame slots and FCMS frame format

The reserved bits - bit7 and bit6 - in the Initialization Mode Identifier(IMI) in Service Code(SC) field is modified to inform the receiver that FCMS frame is for V2V services if needed. Figure 4 shows the modified IMI in the SC field.

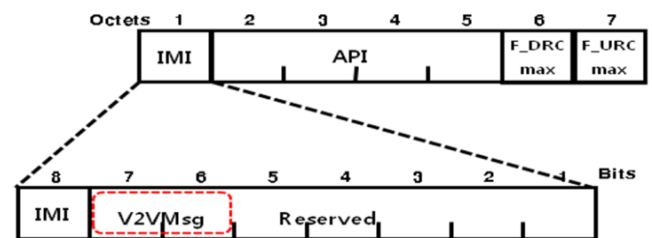


Figure 4. Definition of V2V message field in the SC element in FCMS

Each Status of Data(ST) field in the Control Information (CI)s of SCI fields is modified. It means the following proper MDS or ACTS frame is for V2V communication when the 3-bits value of ST is 101. Table 2 shows the usages of the value of ST. The value 101 of ST originally is reserved bits.

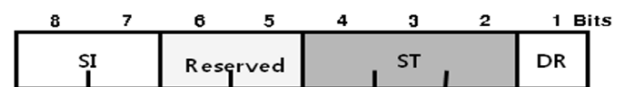


Figure 5. CIs field format : Definition of V2V message field using the ST field in each CI element in FCMS

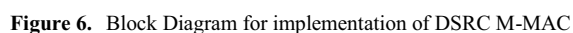
TABLE 2. MODIFIED ST FIELD IN EACH CIs FOR V2V MESSAGES

b4	b3	b2	Description
1	1	1	General data channel
0	1	1	Empty data channel (no slot allocates)
1	0	1	V2V message
0	0	1	Reserved
1	1	0	Reserved
0	1	0	Reserved
1	0	0	Idle signal channel (MPDU set to '1')
0	0	0	Prioritized data channel

C. Block Diagram for implementation of DSRC M-MAC

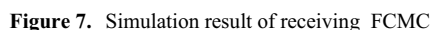
The block diagram for V2V DSRC M-MAC is shown on the Figure 6. The M-MAC block diagram is composed of blocks which are Manchester Decoder, PR(Preamble), FSW(Frame Synchronization Word), CSW(Channel Synchronization Word), the receipt of the FCMC, the receipt of the MDC, the receipt of the ACKC, CRC, analysis of the FCMC, Reception Control, Transfer Control, PLL, Manchester Encoder, Transmission of the FCMC, Transmission of the MDC, Transmission of the ACKC, Transmission of the ACTC, DPRAM, UART Tx, and UART Rx.

To implement them using FPGA, each block is classified into eight modules which are Manchester Encoder, the receipt of the Frames, CRC, analysis of the FCMC, period of transmission, Tx, Control of DPRAM, and PLL.



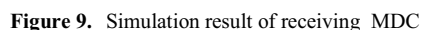
In this chapter, V2V DSRC M-MAC interoperating with the test system is tested. The aim of the test is to verify that the implemented DSRC M-MAC is applied to the DSRC standard. To make sure the test result, ATCT sent by the OBE following FCMC received from the RSE and from other OBE is analysed by through the simulation.

A simulation result of receiving FCMC is shown on the Figure 7. On the operation of the DSRC M-MAC, a received FCMC is stored in DPRAM and analysed, and then the OBE transmits ACTC to access to the RSE. PLL serial data information is indicated due to change the DSRC modem to Tx mode prior to transmit ACTC in signal_out. After transmitting completely, the DSRC modem is re-changed to Rx mode.



A simulation result of transmitting MDC is shown on the Figure 8. A received FCMC is stored in DPRAM and analyzed, and then the OBE transmits MDC to the RSE. The OBE receives ACKC from the RSE as a response to transmitting MDC. PLL serial data information is indicated due to change the DSRC modem to Tx mode prior to transmit

Figure 8. Simulation result of transmitting MDC



A simulation result of receiving MDC is shown on the Figure 9. The DSRC M-MAC receives FCMC and analyzes parameters such as LID, link direction(uplink or downlink) in FCMC. The DSRC M-MAC receives MDC and stores its DPRAM, and then determines through a confirmation of CRC whether MDC contains an error bit. If MDC contains an error, the DSRC M-MAC transfers ACKC to the RSE to inform it. The DSRC M-MAC operation is shown on Figure 10 and 11.



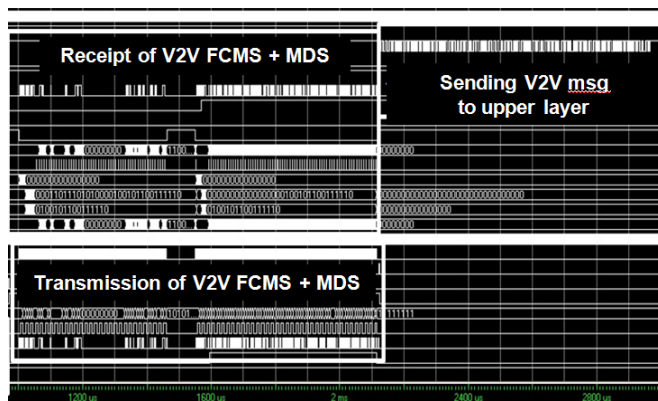


Figure 11. Operation of DSRC M-MAC (2)

IV. CONCLUSIONS

In this paper, the V2V DSRC M-MAC is implemented using the Verilog-Hardware Description Language(HDL). It is possible to build between the OBEs to communicate with each other. The modules and the V2V DSRC M-MAC integrated with them were verified to operate through the result of simulation. The V2V DSRC M-MAC can interoperate to communicate between OBEs and support V2V and V2I communication. The further work is to analyse improvement of network performance by network simulation and to examine by vehicular environments.

ACKNOWLEDGMENT

"This research was supported by the MKE(The Ministry of Knowledge Economy), Korea, under the 'National hrd support program for convergence information technology' support program supervised by the NIPA(National IT Industry Promotion Agency)" (NIPA-2010-C6150-1001-0005)

"This research was supported by the MKE(The Ministry of Knowledge Economy), Korea, under the ITRC(Information Technology Research Center) support program supervised by the NIPA(National IT Industry Promotion Agency)" (NIPA-2010-(C1090-1011-0009))

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