

ASIC Design of 600Mbps 4×4 MIMO Wireless LAN System

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Abstract—This paper shows the design and ASIC implementation of a 802.11n WLANs 4x4 MIMO OFDM PHY transceiver. The system supports the maximum data rate of 600Mbps. The MMSE-SQRD SIC MIMO decoder scheme, which has high BER performance and acceptable hardware cost, is implemented. To meet the required high throughput rate, parallel processing Scrambler/Descrambler, parallel processing BCC, and radix-4 soft-decision Viterbi decoder are implemented. To reduce the hardware cost, the OFDM modulation for both cases 64 and 128 subcarriers is performed by a single mode 128-point (I)FFT per stream. To reduce the system latency, the bit-reversed (I)FFT is implemented. Furthermore, many ideas of combining multi tasks in a single block are implemented to save the hardware resource and the system latency. Our system is implemented in Synopsys CMOS SAED90nm process. The hardware resource cost by the main blocks of the system is exposed. In this paper, the detail description of system architecture is supposed to be useful for people who start to research and/or design the MIMO system.

Keywords: 4x4 MIMO OFDM, 802.11n WLANs, Hardware implement, 600Mbps, PHY Layer.

I. INTRODUCTION

The combination of Multi Input Multi Output (MIMO) wireless technology with the Orthogonal Frequency Division Multiplexing (OFDM) has become one of the most promising techniques for the future of WLANs system. The well-known IEEE 802.11n standard, which is published in 2009 mentions about the MIMO OFDM system, provides a significant increasing on data rate and spectral efficiency [1]. For example, its maximum data rate is 600Mbps. That is about 10 times higher than the maximum data rate of 54Mbps of a Single Input Single Output (SISO) OFDM system defined in IEEE 802.11a standard [2]. However, coexisting with this improvement is a significant increasing on the complexity of the hardware circuit.

Until now, there are many researches focus on implementing the 802.11n chip. Some of them are already available in the market. But there is no chip achieves the maximum data rate of 600Mbps yet. For example, as be shown in [3], an ASIC based MIMO OFDM transceiver achieves the data rate up to 192Mbps. Or in [4], a CMOS SoC prototype of 2x2 MIMO OFDM achieves the data rate up to 205Mbps. In [5], the FPGA based 2x3 MIMO OFDM transceiver achieves the data rate up to 300Mbps. However, to support applications which requires high data transmission rate such as High Definition Television (HDTV) or three dimension television (3D TV), etc., the design of 600Mbps 802.11n chip is necessary.

In this paper, the ASIC implementation of the physical layer (PHY) transceiver of an 802.11n 4x4 MIMO OFDM system is shown. Our system operates at frequency of 160MHz, and supports the maximum data rate of 600Mbps. The verification is taken with the help of IEEE 802.11n transmitter simulation. The hardware circuit is implemented in Synopsys CMOS SAED90nm technology.

This paper is organized as follows: section II shows the system's specification and architecture. Section III focuses on hardware implementation. Section VI shows the ASIC implement's result. And final section V is our conclusion.

II. SYSTEM'S SPECIFICATION AND ARCHITECTURE

A. System's Specification

The specification of our PHY transceiver is shown in table 1. Some important operation parameters are shown in table 2. The structure of the two supported frame formats such as Legacy and Mixed Mode are depicted in Figure 1.

B. System's Architecture

The PHY transmitter's and receiver's architectures are respectively shown in Figure 2 and 3.

TABLE 1. SPECIFICATION OF OUR PHY TRANSCEIVER

Parameters	Supported Values
Frame Format	Legacy / Mixed Mode
Channel Bandwidth	20 MHz / 40 MHz
Modulation and Coding Scheme (MCS)	0 - 31
Guard Interval (GI) duration	0.4us / 0.8us / 1.6us
Number of Spatial Stream (Nss)	1 - 4
Number of Transmitter Antenna	4
Number of Receiver Antenna	4
Carrier Frequency Offset Recovery Range	From +50 ppm to -50 ppm
Forward Error Correction (FEC)	Binary Convolution Code (BCC)

TABLE 2. IMPORTANT OPERATION PARAMETERS

Parameters	Values
Number of (I)FFT tones / or Total of subcarriers per symbol	64 / 128
Number of data subcarriers per symbol	48 / 52 / 108
Number of pilot subcarriers per symbol	4 / 6 / 8
Operation frequency (MHz)	160
Number of clock cycles per symbol duration	576 / 640
Number of up/down sampling factor	4

III. HARDWARE IMPLEMENTATION

A. Parallel Scrambler/Descrambler and BCC

The Scrambler/Descrambler and BCC blocks described in 802.11a standard process the data in serial. To support the data rate up to 600Mbps, the Scrambler/Descrambler, and BCC are designed to process the data in parallel. The Scrambler/Descrambler process 4-bits data per clock cycle and each BCC block process 2 bits data per clock cycle. Those are respectively four times and two times faster than the serial ones described in [2]. In our implementation, where all blocks operate at 160 MHz, the Scrambler/Descrambler supports the data rate up to $4\text{bits} \times 160\text{MHz} = 640\text{Mbps}$, and two BCC blocks support the data rate up to $2 \times 2\text{bits} \times 160\text{MHz} = 640\text{Mbps}$.

B. Single Mode 128-Point Bit-reversed IFFT/FFT

The Legacy and 20MHz Mixed Mode formats require a 64-point (I)FFT to perform the multicarrier modulation, while the 40MHz Mixed Mode format requires a 128-point (I)FFT one. To support all these cases, each stream needs a multi-mode (I)FFT which be able to operate at either 64-point or 128-point modes. Or two (I)FFTs are required per stream, one is 64-point type and the other is 128-point type. In the first option, the multi-mode (I)FFT is more complex and thus costs time and hardware resource for designing and implementing than the 128-point (I)FFT does. In the second option, using two (I)FFT per stream is not good in term of hardware cost.

In our solution, a single mode 128-point IFFT/FFT per stream is implemented. For 64-subcarrier symbol case, the first 32 subcarriers of data are mapped into the first 32 points, while the remained 32 subcarriers are mapped into the last 32 points (from point 96 to 127) of the 128-point IFFT. The middle points from 32 to 95 of IFFT are inserted by 0. At the receiver side, the 64 subcarriers of received data are located at the first 32-points and the last 32 points of 128-point FFT's output. Value of the FFT's outputs from point 32 to 95 are expected to be 0 and ignored.

In addition, the bit-reversed (I)FFT is implemented to reduced the system's latency by $266 - 137 = 129$ clock cycles. In which, 266 and 137 clock cycles are respectively the latency of the bit-normal and bit-reversed (I)FFT.

C. Multi-mode Interleave/Deinterleave

Interleave/Deinterleave is used to reduce the effect of burst error into the transmitted data, thus improve the performance of the Viterbi decoder. The final purpose is to increase the BER performance of the system. Our multi-mode Interleave/Deinterleave performs three permutations defined in 802.11a and 802.11n standards. The multi mode term means that it supports many operation modes such as BPSK, QPSK, QAM16, QAM64 mapping types; Legacy, 20MHz Mixed Mode, 40 MHz Mixed Mode formats, etc.

In addition to performing three permutations, the Interleave blocks do the IFFT shift. The Deinterleave reorders the bit-reversed output of the FFT, and shifts the data back to its original position, which opposites to the IFFT shift. These supplement tasks are done by simply changing the read address of the Interleave/Deinterleave's RAM, and thus do not

cost more the hardware resource. As a result, hardware cost and latency of the system is saved because there is no need to implement a dedicated IFFT shift, FFT reordering, or IFFT shift back. The design of our De-Interleave block is shown in [6].

D. MIMO Decoder

MIMO decoder is the most important and complex part of the MIMO system. In our knowledge, the Maximum Likelihood Detection (MLD) algorithm based MIMO decoder achieves the best BER performance. In tradeoff, this method costs too much hardware resource as compare with the others such as Linear Minimum Mean Square Error (LMMSE), or QRD-MMSE, etc.

In our system, in case of multi spatial streams, in which the number of spatial streams is larger than 1, the MMSE Sorted QR Decompose (SQRD) Successive Interference Cancelling (SIC) MIMO Decoder scheme is implemented. As shown in [7], MMSE SQRD SIC achieves better BER performance and costs lower hardware resource than the LMMSE does. According to our simulation result (Figure 4), the SQRD-MMSE SIC respectively achieves about 9dB and 12dB higher than those of the QRD-MMSE SIC and LMMSE. Our SQRD block is designed by using the modified Gram-Schmidt algorithm with pipelining and recursive processing [8] for saving hardware resource.

In case of single spatial stream, the Maximum Ratio Combining (MRC) method is implemented. In this case, MRC has better BER performance than the SQRD-MMSE SIC does. According to this method, if X is the transmitted data; Y_1, Y_2, Y_3, Y_4 and H_1, H_2, H_3, H_4 are respectively the received data and estimated channel of stream 1, 2, 3, and 4 at frequency domain. Then, X is recovered by following

$$\text{equation: } X = \frac{Y_1 H_1 + Y_2 H_2 + Y_3 H_3 + Y_4 H_4}{H_1^2 + H_2^2 + H_3^2 + H_4^2} \quad (1)$$

The MRC and SQRD-MMSE SIC are implemented by sharing the common hardware resource.

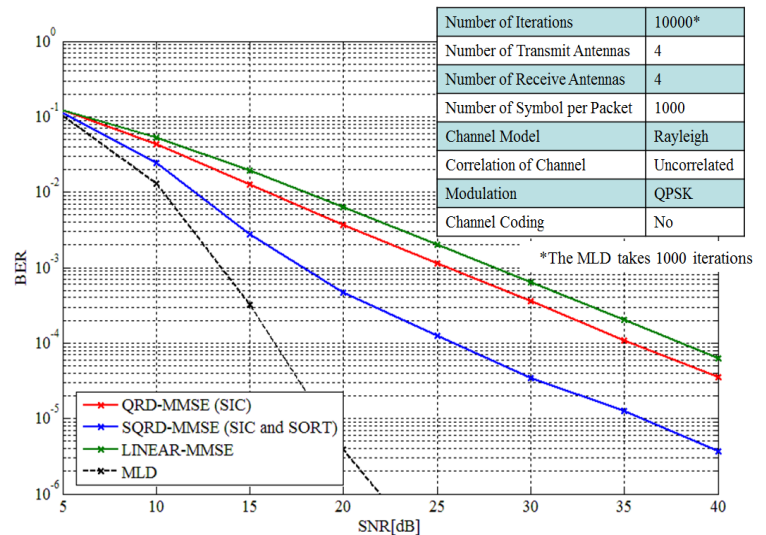


Figure 4. BER simulation results

E. Radix-4 Soft-decision Viterbi Decoder

To be able to support the data rate of $300\text{Mbps} \times 2 = 600\text{Mbps}$, each Viterbi Decoder has to process four data per clock cycles, which cannot be done by Radix-2 Butterfly architecture. In our system, the radix-4 soft-decision Viterbi decoder [9] is implemented. The soft-decision type is used to increase the BER performance.

F. Multi-tasks GI Inserter (GII)

The main purpose of this block is to prepend the Guard Interval (GI) to each OFDM symbol. Besides, the GII block is designed to do the supplement tasks such as reordering the bit-reversed output of the IFFT, performing the time cyclic shift for non-HT preamble and Legacy DATA, and up sampling the data by a factor of 4.

These supplement tasks do not increase the hardware resource of the GII. They are implemented by simply changing the way of writing, reading the RAM of the block. As a result, the hardware resource and latency, which expected to cost by the supplement tasks, are removed.

IV. ASIC RESULTS

Our system is implemented in Synopsis SAED90nm process. The hardware resource cost by the most complex blocks is shown in table 3.

The Comb-Resource column shows the number of K gates of the combinational circuit. The Total Area column shows the total of combinational, non-combinational and net area in term of mm^2 . The external RAM column shows the amount of required external RAM.

According to the results, the total chip size is expected about 13mm^2 plus 200 Kbits of external RAM. And the five blocks such as Frame Sync, MIMO Decoder, Phase Tracking, Viterbi Decoder, and FFT/IFFT cost most hardware resource of the system. Thus, the researches on optimizing these blocks play an important role on reducing the chip size.

TABLE 3. ASIC IMPLEMENT'S RESULTS

Block name		Comb-Resource [Kgate]	Total Area [mm^2]	External RAM [Kbits]
4 x Interleave / 4 x De-Interleave		38.8 / 67	0.46 / 1.08	0
Spatial Mapping		91	0.64	0
4 x IFFT / 4 x FFT		170 / 191	1.28 / 1.41	0
4 x GII / 4 x GIR		3.3 / 1.7	0.047 / 0.026	36 / 18
AGC		41.7	0.351	0
CFO		38	0.306	0
Frame Sync.		445	4.016	0
Channel Estimation		23.5	0.223	72
Phase Tracking		205	1.509	0
MIMO decoder	SQRD	179	2.02	100
	Equalizer +SIC	77	0.675	0
2xViterbi Decoder		190	2.1	0

V. CONCLUSION

In this paper, the design and ASIC implement's results of an 802.11n 4x4 MIMO OFDM system are shown. The implements to deal with high data rate, system latency, and hardware resource issues are exposed. The system's BER performance is maximized by implementing many blocks such as BCC, soft-decision Viterbi Decoder, Interleave/DeInterleave, SQRD-MMSE SIC and MRC MIMO Decoder. The detail description about the system architecture is supposed to be useful for people who start to research and/or design the 802.11n MIMO OFDM system.

At the time of submitting this paper, we finished verifying the transmitter side and in progress of verifying the receiver side. An FPGA prototype of the system is supposed to be available by the end of 2011.

The research showed in this paper is planned to be the first version of the 600Mbps 4x4 MIMO OFDM system. Based on that, our research is enhanced for reducing the chip size and increasing the BER performance for the next versions of the system.

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