

A Fully Integrated Pulsewidth Modulator for Class-S System

Bonghyuk Park, Jaeho Jung

Mobile RF Research Team, ETRI, Daejeon, South Korea

bhpark@etri.re.kr

Abstract— Switch-mode power amplification of varying envelope signal has gained influence in the mobile communication system because of its high linearity and efficiency. A fully integrated pulsewidth modulator (PWM) has been presented in this paper for switch-mode power amplifier. The HBT BiCMOS design of pulsewidth modulator circuit is applied to the LTE(Long Term Evolution) frequency range, which converts digitally modulated 955 MHz RF signal with a clock rate of 2.4 GHz. The modulator has been designed in a 0.25- μm SiGe-BiCMOS technology.

Keywords— Pulsewidth Modulator, Class-S, High efficiency, BiCMOS

I. INTRODUCTION

In recent, high data rate transmission of varying envelope signal with high peak-to-average ratio (PAPR) is required, therefore energy efficiency of base stations become increasingly more and more significant. The high efficiency power amplifiers (PAs) are mostly focusing on switch-mode operation [1]-[3]. One of the candidates of the switch-mode amplification system is Class-S concept as shown in Fig. 1. This transmitter consists of PWM, Switching PA, and Bandpass filter. There are mainly two kinds of modulator which non-constant input signal is converted to two state digital signal ; delta-sigma modulator (DSM) and PWM. Usually, continuous-time (CT) BPDSM is used for high speed modulator to convert input RF signal to single-bit digital-RF sequence [4]. In order to design the DSM, the quantization noise must be filtered after PA. However, an RF PWM modulator does not suffer from quantization noise and is, therefore, more useful for standards such as long term evolution (LTE) [5]. The digital signal is then amplified by

means of a highly efficient power switching stage. The non-constant input signal is reconstructed using bandpass filter at the output of the switching stage. In this paper, the 955 MHz carrier input PWM system and circuit are presented.

This paper is organized as follows. Section I provides a general introduction of high efficiency switching power amplifier. Section II presents the circuit design and implementation of triangle signal generator and comparator. In Section III, full RF pulse-width modulator simulation results and layout are discussed. Section IV gives the conclusions.

II. CIRCUIT IMPLEMENTATION

The PWM is composed of two main functional blocks: a triangle signal generator and a comparator. The schematic of signal generator without biasing circuit is shown in Fig. 2. Differential sinewave clock signals are injected through CLK, CLKB nodes of 300mV peak at each node. The capacitor C1 converts the rectangular-shaped current shown in Fig. 3 to triangle-shaping voltage signal following equation (1), then 2nd stage generates the pure triangle signal. The direction of the charging current is alternately switched, so that the voltage across the capacitor rises and falls nearly linear with time. The single-ended OUT signal is compared with non-constant input in comparator block.

$$v(t) = v(t_0) + \frac{1}{C} \int_{t_0}^t i(t) dt \quad (1)$$

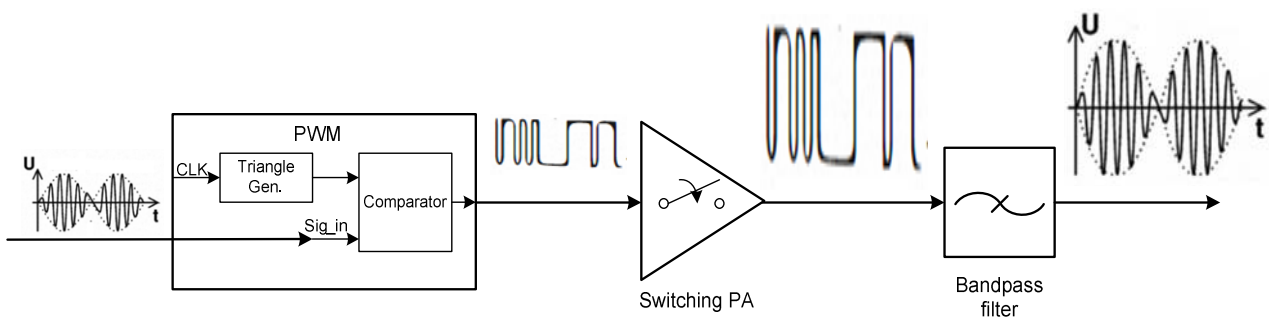


Figure 1. Class-S transmitter

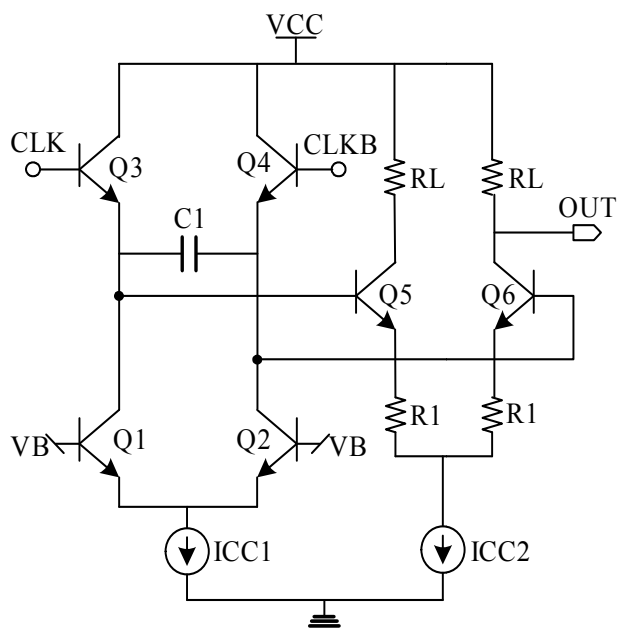


Figure 2. Triangle signal generator

The differential output results of triangle signal generator are shown in Fig. 4. In contrast to the sawtooth reference signal, the triangular signal does not have steep falling edges, which save a considerable amount of bandwidth.

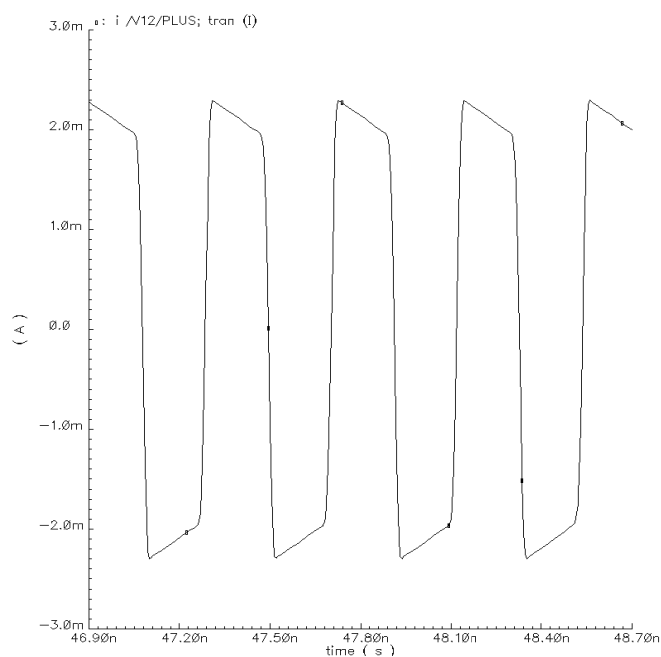


Figure 3. Current characteristic through the Capacitor

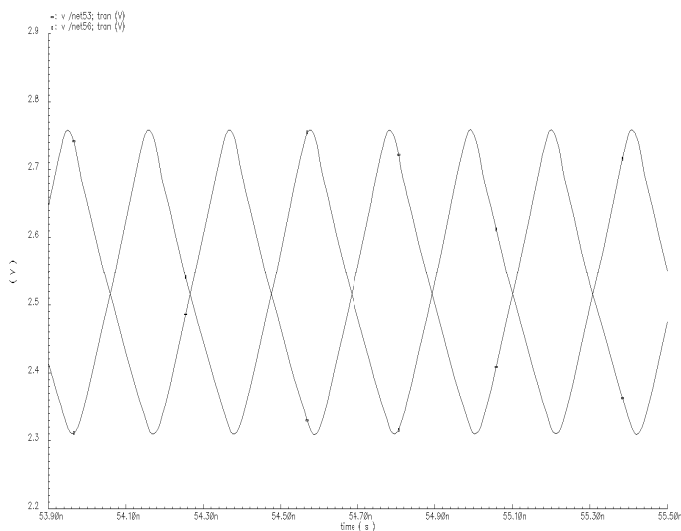


Figure 4. The output characteristic of triangle signal generator

Comparator block compares the reference signal (triangle signal) with non-constant input signal. The circuit of comparator is shown in Fig. 5, which makes the digitally pulse output at OP and ON nodes as shown in Fig. 6. The single-ended voltage swing is about 724 mV peak-to-peak.

The sinewave input signal is entered at node SIG_IN and triangle reference signal is injected at node TRI_IN. Reference signal is greater than the input signal then the output is “High” state and vice versa as shown in Fig. 7. Comparator is composed of 2-stage differential amplifier topology. It draws 16.5 mA current at 3.3 V supply.

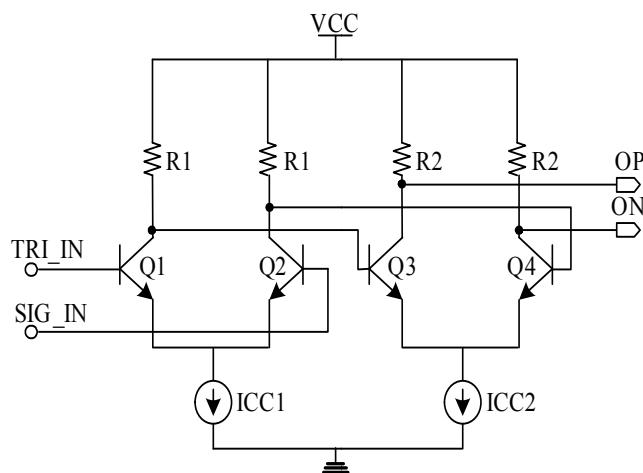


Figure 5. Comparator circuit schematic

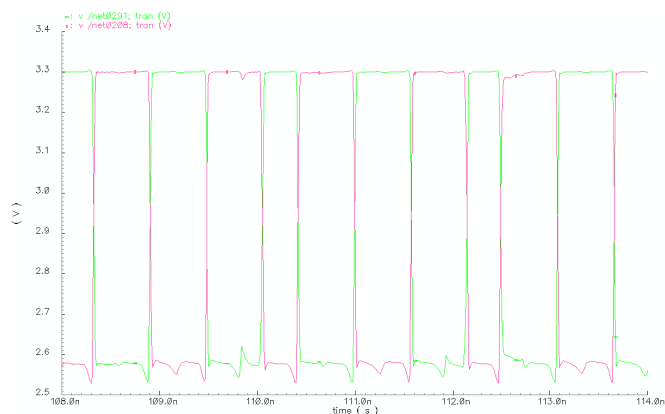


Figure 6. Comparator output signal

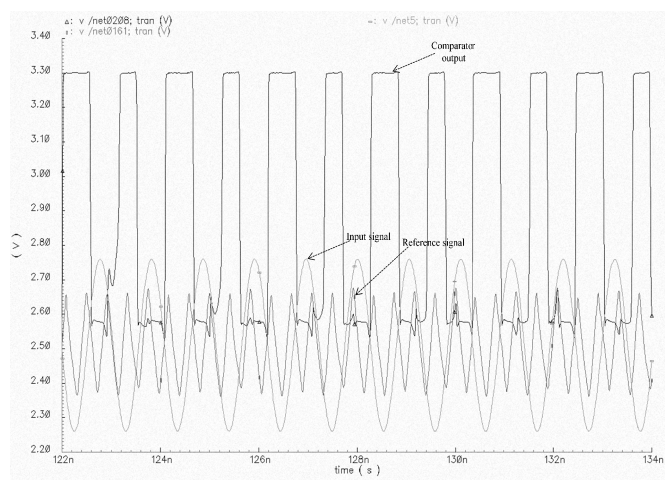


Figure 7. Comparison of the input signal with reference

III. FULL PWM IMPLEMENTATION

Full chip PWM is composed of triangle signal generator, comparator, and buffer for $50\ \Omega$ load impedance as shown in Fig. 8. In order to drive the low impedance loads, the buffer consists of common source (CS)-source follower-CS cascaded stages.

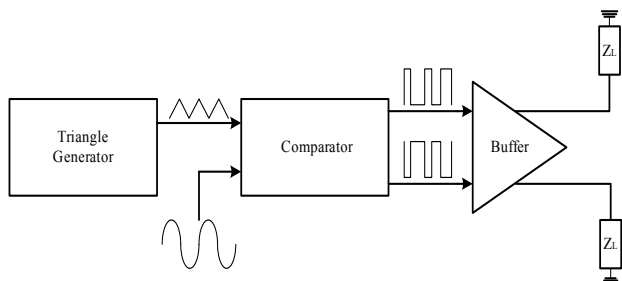


Figure 8. Full PWM architecture

The modulator has been designed in a $0.25\text{-}\mu\text{m}$ SiGe BiCMOS technology. The micrograph of full chip PWM is shown in Fig. 9. The size of this chip is $610\ \mu\text{m} \times 510\ \mu\text{m}$ including the PADs. The PWM consumes $62.7\ \text{mA}$ at $3.3\ \text{V}$ supply voltage including the buffer.

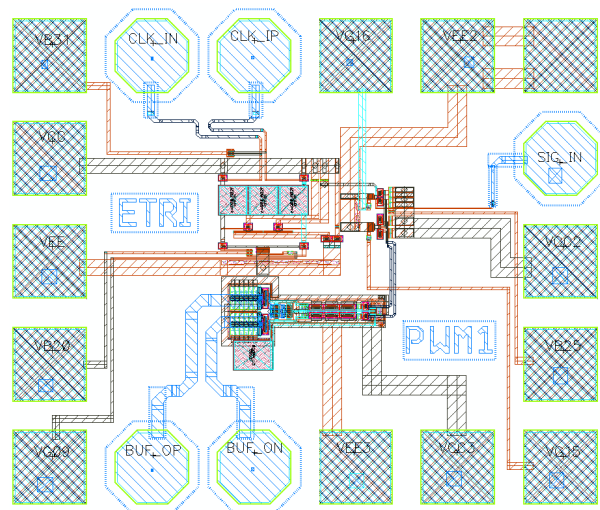


Figure 9. The photograph of full chip PWM

In Fig. 10, the time domain output signal of the PWM is shown. The peak-to-peak voltage amplitudes of $697\ \text{mV}$ are obtained at single-ended output node. In the transient response characteristics, the oversampling ratio of three can be observed, as the pulsewidth pattern repeats after every three clock cycles. In this case the input signal frequency is $955\ \text{MHz}$ at clock of $2,865\ \text{MHz}$.

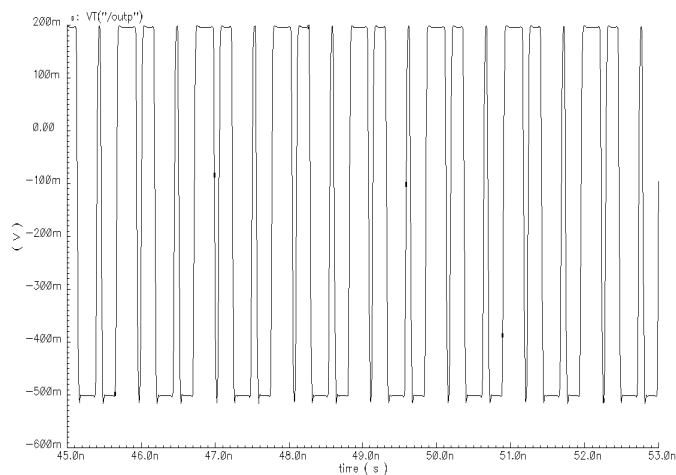


Figure 10. Output signal of PWM in transient response

IV. CONCLUSIONS

A fully integrated PWM circuit and post-layout simulation results are presented. Two digit digitally pulse is applied for

high efficiency switching power amplifier. This system will be used for mobile green basestation.

ACKNOWLEDGMENT

This work was supported by the IT R&D program of MKE/KEIT [10035173, Research on the Class-S base-station power amplifier technology for future mobile communications]

REFERENCES

- [1] H. Kobayashi, J. Hinrichs, P.M. Asbeck, "Current-Mode Class-D Power Amplifiers for High Efficiency RF Applications," *IEEE MTT-S International Microwave Symposium Digest*, May 2001, pp. 939-942.
- [2] T. Hung, J. Rode, L.E. Larson, P.M. Asbeck, "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," *IEEE MTT-S International Microwave Symposium Digest*, May 2007, pp. 1091-1094.
- [3] R. Leberer, R. Reber, M. Oppermann, "An AlGaIn/GaN Class-S Amplifier for RF-Communication Signals," *IEEE MTT-S International Microwave Symposium Digest*, June 2008, pp. 85-88.
- [4] Hyungjung Kim, Jin-up Kim, Jaehyung Kim, Hongmei Wang and Insung Lee, "RF Band-Pass Sampling Frontend for Multiband Access CR/SDR Receiver," *ETRI Journal*, vol. 32, no. 2, April 2010, pp. 214-221.
- [5] Michael Nielsen and Torben Larsen, "A 2-GHz GaAs HBT RF Pulsewidth Modulator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 2, February 2008, pp. 300-304.