

Comparative Analysis of Single-ended and Differential Receiver Modules in 0.13 μm CMOS technology

Jamshid Sangirov, Ikechi Augustine Ukaegbu, Nga T.H. Nguyen, Tae-Woo Lee, Mu-Hee Cho, and Hyo-Hoon Park

Photonic Computer Systems Lab., Electrical Engineering Dept., KAIST, Daejeon, Korea 305-701

jamshid@kaist.ac.kr

Abstract— Designing of a small-area optical receiver (Rx) may require intuitive solutions, such as building single-ended Rx and utilizing some of the advantages of differential Rx. Optical Rx should provide sufficient gain and frequency operation for feeding to subsequent blocks including clock and data recovery circuit (CDR) and/or Serializer and Deserializer (SerDes) with reduced size for building compact optical Rx modules. Therefore, we have designed single-ended and differential Rx modules and analyzed their performance comparatively in terms noise, power, size, and gain. Optical Rx chips have been fabricated using 0.13 μm complementary metal-oxide-semiconductor (CMOS) technology to demonstrate performance of optical Rx modules. The fabricated single-ended Rx chip core size is equal to 0.035mm² and consumes power of 10.3mW at 1.3V. The fabricated differential Rx chip core size is equal to 0.135 mm² and consumes power of 65.8mW at 1.3V. The input-referred noise (IRN) of single-ended and differential optical Rx chips is equal to 34pA/ $\sqrt{\text{Hz}}$ and 30pA/ $\sqrt{\text{Hz}}$, respectively. The 3-dB bandwidth of differential and single-ended Rx optical modules is equal to 2.5GHz and 3GHz, respectively.

Keywords— single-ended receiver, small-area circuit design, bandwidth improvement, differential receiver, receiver module

I. INTRODUCTION

The recent rapid growth in data traffic between chip-to-chip and board-to-board is causing dramatic increase in capacity of signal transmission in communication technology equipments such as servers, routers, and storage systems. Conventional, electrical transmission has poor power efficiency at high data rates [1]. Optical interconnection has lower power transmission at high data rates and has negligible insertion loss with inner-channel crosstalk for multi-channel optical link. Hence, optical interconnection is being widely utilized in high data rate video and data transmission systems [2]. However, there are multiple design challenges in designing optical-to-electrical (o/e) and electrical-to-optical (e/o) converting IC circuits including their performance, size and power dissipation. Where optical Rx chip with photodiode (PD) plays as a front-end Rx of the optical signal and amplifies the electrical signal after converting it from optical signal. And the optical Tx circuit with laser diode converts electrical signal to optical signal. The low-cost 850 nm vertical cavity surface emitting lasers (VCSEL) diodes are widely used for

short-reach optical interconnect applications. CMOS compatible silicon photo detector PDs demonstrate reasonable responsivity in the 850 nm wavelength which can easily be integrated and matched for 850 nm VCSEL transmitters.

As the technology developing and miniaturization of CMOS technology is pushing the design limits to build even smaller chips. It is important to design compact optical Rx circuits for high-speed operation to reduce the signal propagation loss and reduce the active area used for chip design. Thus, designing of small-area optical Rx modules may require intuitive solutions, such as utilizing some of the advantages of differential Rx in designing of a single-ended Rx modules. Optical Rx chip should provide a sufficient gain and frequency operation with reduced size for feeding the signal to post-processing blocks such as CDR and/or SerDes [3-4]. However, there are performance trade-offs between single-ended and differential Rxs and our focus is to show the advantages of the single-ended Rx. Therefore, we have designed single-ended and differential receivers and analysed their performance comparatively in terms noise, power, size, and gain.

II. DESIGN OF SINGLE-ENDED AND DIFFERENTIAL RX

The single-ended Rx consists of input stage, gain stage and output buffer, where differential Rx consists of transimpedance amplifier (TIA), limiting amplifier (LA) and output buffer. The inductor-less design topologies has been utilized for designing both single-ended and differential optical Rxs.

A. Design of Single-ended Rx

Figure 1 shows the block diagram and schematic of single-ended Rx. The Rx consists of an input stage, A1, a gain stage, A2 and an output buffer. The main bandwidth limitation of conventional optical front-end Rx is at the input stage because of input PD parasitic capacitance. To reduce input impedance and eliminate input parasitic capacitance from bandwidth determination, regulated-cascode (RGC) topology with shunt feedback [5] has been adopted as shown in Figure 1(b). However, the gain of RGC alone is not enough to drive other circuits connected to Rx such as CDR and/or SerDes. To improve Rx gain further several stages of common source (CS)

transistors have been utilized to increase the gain. Using only cascaded CS stages may reduce the frequency operation of Rx circuit. Therefore, the bandwidth improvement should be utilized to increase the frequency operation. One of the widely used method for bandwidth improvement is using active (negative) feedback as a replacement to large size inductors and often utilized in designing of differential Rx for increasing bandwidth of LA and automatic gain control (AGC) amplifiers [6-7]. Hence, the same active feedback system can be effectively applied to increase the gain and improve the frequency operation of single-ended Rx [8]. As shown in Figure 1(c) active feedback has been used to increase the bandwidth and gain of the single-ended Rx.

Using more amplifying stages to built and Rx can increase the overall power consumption of Rx. Therefore, device sizes of transistors have been reduced to reduce the power consumption of Rx. Reducing the sizes of active devices should be compensated for the active feedback system as well. However, reducing the size of active devices excessively may reach the limit of active devices for feedback amplifiers, M_{f1} and M_{f2} . Hence, the R_{f1} and R_{f2} resistors are utilized to reduce feedback amount equivalent to the device size proportions as shown Figure 1 (c).

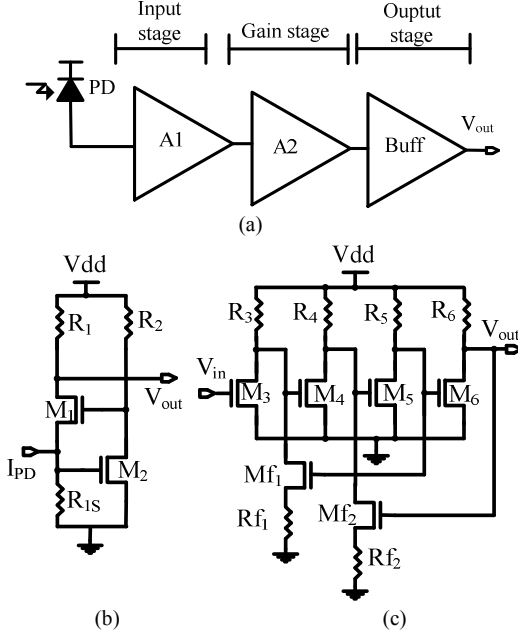


Figure 1. (a) The block diagram of single-ended Rx, (b) RGC circuit and (c) gain stage of single-ended Rx.

When PD is reverse biased, with cathode positive, the response time reduces. This happens due to increase in depletion layer and decrease in junction capacitance of PD. However, this may increase the IRN noise, which may degrade system performance dramatically. To compensate for noise improvement, the input stage of the Rx should have better noise immunity. Here, RGC input stage can give better noise isolation. The input impedance of RGC stage shown in Figure 1(b) is given by:

$$Z_{IN,RGC} = 1/(g_{m1}(1 + g_{m2}R_2)) \quad (1)$$

where $(1 + g_{m2}R_2)$ is the voltage gain of RGC feedback. The input impedance of RGC is $(1 + g_{m2}R_2)$ times smaller comparing to common-gate stage (CG). Thus, the RGC isolates the input parasitic capacitance, C_{PD} , better than CG stage. Hence, RGC input stage behaves like CG stage with large transconductance G_m :

$$G_m = g_{m1}(1 + g_{m2}R_2). \quad (2)$$

Due to its large gain, RGC input stage can be considered as a single pole-system and 3-dB bandwidth is given by:

$$f_{3dB,RGC} = \frac{1}{2\pi R_1 C_{d1}}, \quad (3)$$

where C_{d1} is the drain capacitance of M_1 [5]. While 3-dB frequency of CG input stage is given by:

$$f_{3dB,CG} = \frac{g_{m1}}{2\pi(C_{pd} + C_{s1})}, \quad (4)$$

where C_{s1} represents the source capacitance of M_1 . As can be seen from eq. (3) and eq. (4), that RGC can give higher bandwidth than CG stage.

Gain stage of single-ended Rx can be represented by an amplifier with third-order feedback as shown in Figure 2.

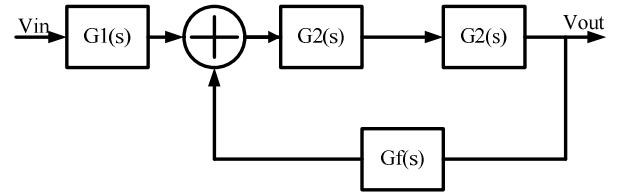


Figure 2. The third-order negative feedback system.

Third-order feedback utilized in single-ended Rx can be explained by its transfer function. The transfer function of active feedback system can be characterized by :

$$H(s) = \frac{G1(s) \cdot G2(s) \cdot G3(s)}{1 + G2(s) \cdot G3(s) \cdot Gf(s)}, \quad (5)$$

the gain of each stage can be approximated:

$$G1(s) = G2(s) = G3(s) = \frac{GmR}{1 + sRC}, \quad (6)$$

$$Gf(s) = \frac{GmfR}{1 + sRC}, \quad (7)$$

where R and C are resistive and capacitive loads of amplifying stages and negative active feedback shown in Figure 1(c). The 3-dB bandwidth increase of active feedback of M_{f1} and M_{f2} has been included in the transfer function of the gain stage and the equation is given as:

$$\frac{V_{out}}{V_{in}} = \frac{G_3(s)G_4(s)G_5(s)G_6(s)}{1 + G_4(s)G_5(s)Gf_1(s) + G_5(s)G_6(s)Gf_2(s)} \quad (8)$$

$$= \frac{G^4(s)}{1 + 2G^2(s)Gf(s)}$$

where $G_5(s) = G_6(s) = G_7(s) = G(s)$. The size change of feedback $Gf(s)$ of the gain stage affects the frequency response and increasing $Gf(s)$ results to high peaking in higher frequencies, hence the frequency operation would be increased by reducing the gain in lower frequency [6, 8].

B. Design of differential Rx

The differential optical receiver topology is shown in Figure 3. It is based on replica TIA, where TIA topology has been built similar to single-ended Rx input and gain stages. The TIA output is connected to LA.

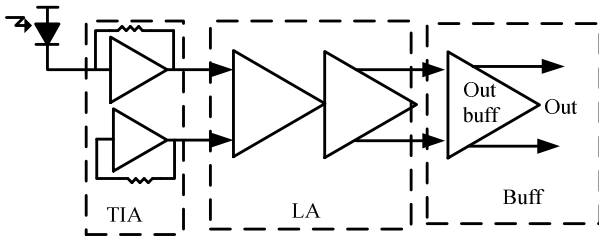


Figure 3. Figure 6. The topology of differential optical receiver.

The inductor-less design has been utilized to LA [5], where active feedback has been applied to increase the frequency operation of the optical receiver. The Limiting Amplifier (LA) has several gain stages and uses active feedback to enhance the frequency operation, and contains 50Ω matched output buffer as shown in Figure 4. The gain cell consists of simple current sharing differential gain cells.

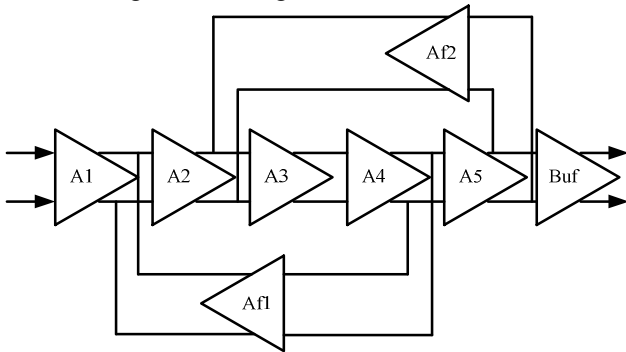


Figure 4. The block diagram of LA.

The LA transfer function can be explained the same way as for the third-order negative feedback:

$$H(s) = \frac{G1(s) \cdot G2(s) \cdot G3(s) \cdot G4(s)}{1 + G2(s) \cdot G3(s) \cdot G4(s) \cdot Gf(s)} \quad (9)$$

The gain of each stage can be approximated

$$G1(s) = G2(s) = G3(s) = G4(s) = \frac{GmR}{1 + sRC} \quad (10)$$

$$Gf(s) = \frac{GmfR}{1 + sRC} \quad (11)$$

And final substitution of eq. (10) and (11) to (6) gives us the following

$$H(s) = \frac{G^4 mR^4}{(1 + sRC)^4 + G^3 mGmfR^4} = \frac{A_0^4}{(1 + s/\omega_0^4) + A_0^3 \beta} \quad (12)$$

where $\omega_0 = 1/RC$, $A_0 = GmR$ and $\beta = GmfR$. Similarly, the size change of feedback β of the gain stage affects the frequency response. However, in order to reduce the power dissipation of LA the feedback system should be reduced proportionally to the amplifier stages.

III. DISCUSSION AND SUMMARY

The single-ended and differential optical Rx modules have been designed and fabricated in $0.13\mu\text{m}$ CMOS technology to demonstrate Rx operation. The comparison of single-ended and differential optical Rx modules were based on simulated and measured results and their overall performance in terms noise, power, size and gain. The photograph of single-ended and differential optical Rx modules with PD and single layer capacitor mounted on printed circuit board (PCB) are shown in Figure 5. The PD is connected to 3.3 V with bypass 100 nF capacitor for both Rx modules. The Rx modules are connected to 1.3 V voltage supply with 0.1 μF of bypass capacitors.

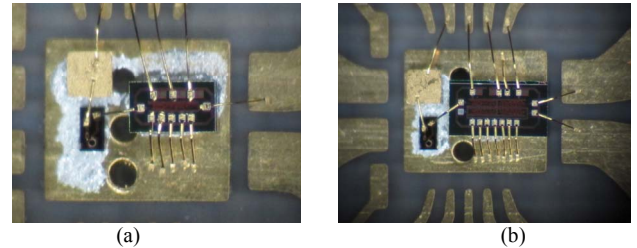


Figure 5. The photograph of (a) single-ended Rx module and (b) differential Rx module.

A. Gain, bandwidth and noise

Figure 6 show the simulated gain of Rx chips as well as measured S21-paramters of Rx modules. The simulated gains are 65dB Ω with 3-dB bandwidth of 6.4GHz and 86dB Ω with 6.2GHz for single-ended and differential Rx modules, respectively as shown in Figure 6(a) and (b). The 3-dB bandwidth of single-ended optical Rx module is equal to 3GHz as shown in Figure 6(c). The 3-dB gain of differential optical receiver module is equal to 2.56GHz as shown in Figure 6(d). The single-ended Rx module has slightly higher bandwidth comparing to differential Rx module. This happens due to the replica based TIA has been utilized in differential Rx design, where from single-ended to differential conversion is required. Thus, the bandwidth of differential may show relatively smaller bandwidth comparing to single-ended Rx design.

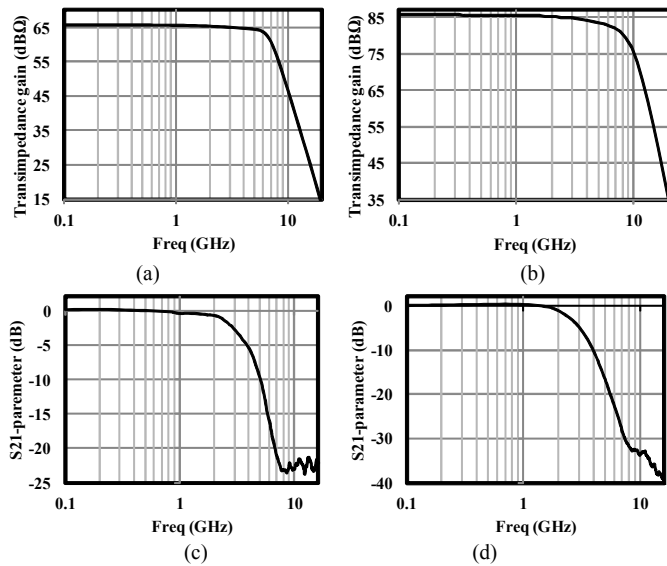


Figure 6. The simulated transimpedance gain and measured S21-parameter (a) single-ended Rx chip, (b) differential Rx chip of (c) single-ended Rx module and (d) differential Rx module.

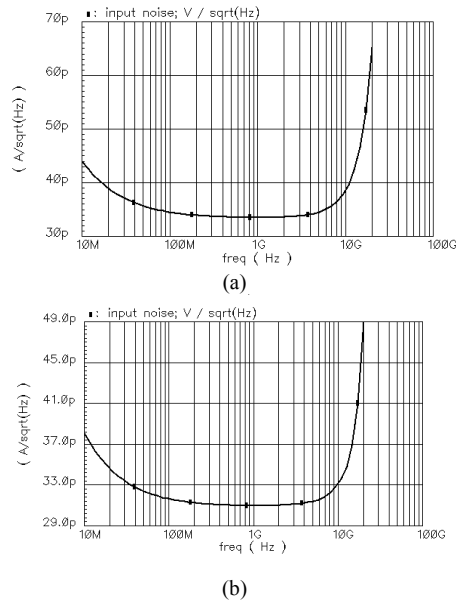


Figure 7. The simulated IRN of (a) single-ended Rx and (b) differential Rx.

The simulated IRN noises of single-ended and differential Rx chip are shown in Figure 7(a) and (b). The IRN noise of single-ended Rx chip at 3-dB bandwidth is equal to $34\text{pA}/\sqrt{\text{Hz}}$, while the IRN noise of differential noise of differential Rx at 3-dB bandwidth is equal to $30\text{pA}/\sqrt{\text{Hz}}$. The output integrated noises of the single-ended and differential Rx modules are shown in Figure 8, which has been measured with disconnecting the input of Rx modules (optical light are not applied to the input of Rx modules). The output integrated noise of single-ended and differential Rx modules are equal to 0.548mV and 0.453mV , respectively, by subtracting the oscilloscope noise of 0.1 mV the noise of Rx modules

becomes 0.458mV and 0.353mV for single-ended and differential Rx modules, respectively. Since, the differential Rx has a common mode rejection, thus the differential Rx has better immunity to noise. Therefore, the simulated and measured noise shows better results for differential comparing to single-ended Rx design.

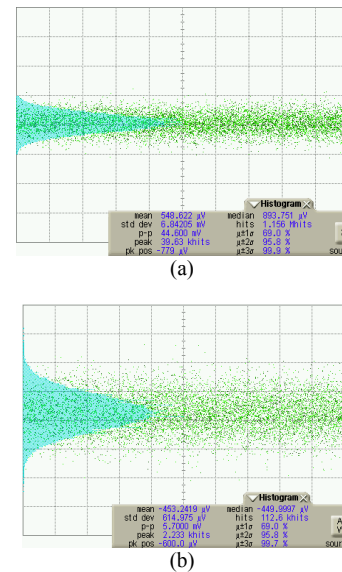


Figure 8. The measured output integrated output noise of (a) single-ended Rx module (b) differential Rx module.

B. Power, area and performance

The single-ended Rx core size is 0.035mm^2 with recorded power consumption of 10.3mW at 1.3V . While differential Rx core size is 0.135mm^2 with recorded power consumption of 65.8mW at 1.3V . Hence, the power consumption of single-ended Rx comparing to differential Rx is smaller.

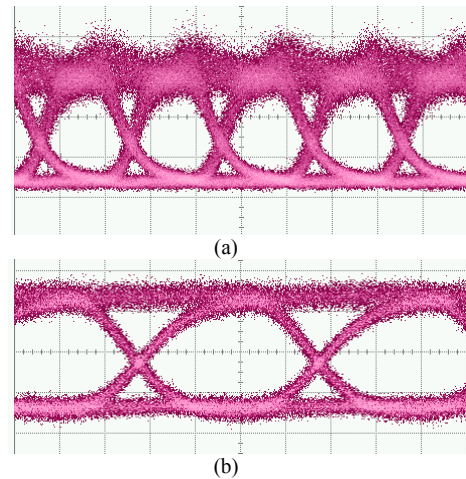


Figure 9. The measured eye-diagrams of (a) single-ended optical Rx module $13.9\text{mV}/\text{div}$, $100\text{ps}/\text{div}$ at 2.5 Gbps (b) differential optical Rx module, $10\text{ mV}/\text{div}$, $50\text{ps}/\text{div}$ at 2.5 Gbps .

The measured eye-diagrams of single-ended and differential optical Rx modules are shown in Figure 9 at 2.5 Gbps with input power of -3dBm . The root mean square

(RMS) jitter of single-ended Rx is equal to 75 ps with rise/fall times of 200/300 ps (from 10% to 90%), respectively. The RMS jitter of differential Rx is equal 60ps with rise/fall times of 300/298 ps (from 10% to 90%), respectively. The measured BER vs data rate graph of single-ended and differential Rx modules are shown in Figure 10 with input power of -3dBm. From the graph it can be seen that the BER of single-ended Rx module is degrading faster comparing to differential Rx module for increase of data rate. This could be due to the single-ended topology has relatively higher noise. When high frequency waves are travelling through differential Rx the common mode rejection helps the reduction of noise [5], since data is differential and noises from negative and positive channels cancels each other.

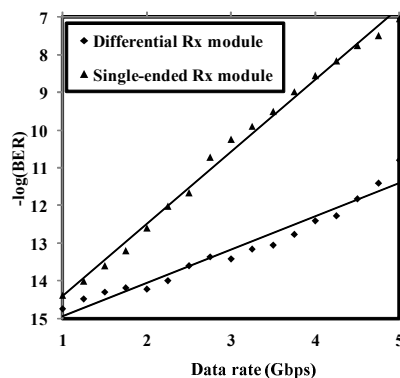


Figure 10. Measured BER vs data rates.

C. Summary of results

Table 1 summarizes the single-ended and differential Rx's. From these results we can draw some concluding points that the differential topology has shown better results in dynamic characteristics with better BER and eye-diagram. However, the single-ended topology resulted to smaller power consumption, smaller-area with slightly higher bandwidth and smaller gain. The single-ended topology may produce less heat while occupying the smaller area with smaller power consumption. These advantages can make the single-ended topology more attractive for optical Rx design. Since, the miniaturization of CMOS technology is pushing the design limits to design even smaller chips.

TABLE 1. SUMMARY OF SINGLE-ENDED AND DIFFERENTIAL RXS

Rx type	Chip size (mm ²)	Power (mW)	Rx chip		Rx module BW (GHz)
			Gain (dBΩ)	BW (GHz)	
Single-ended	0.035	10.3	65	6.4	3
Differential	0.135	65.8	86	6.2	2.56

Hence, for designing small-area optical Rx modules, it might be required to utilize some of the advantages of differential Rx to design a single-ended Rx module with smaller area and smaller power consumption, while providing sufficient gain and frequency operation to be able to feed to

CDR and/or SerDes functional blocks and reduced size for designing optical Rx modules.

IV. CONCLUSIONS

The single-ended and differential Rx chips have been designed and fabricated in 0.13μm CMOS technology in order to analyse their performance comparatively in terms noise, power, size and gain. The single-ended Rx has been built with small-area, low-power consumption by utilizing some of the advantages of differential Rx and the performance of single-ended Rx were compared with differential Rx. The single-ended Rx die has core of 0.035 mm² with power consumption of 10.3mW at 1.3V. The differential Rx die has core of 0.135 mm² with power consumption of 65.8mW at 1.3 V. The input-referred noise of single-ended Rx is 34pA/√Hz and differential Rx is 30pA/√Hz. The differential optical receiver has 3-dB Bandwidth of 2.5 GHz and single-ended optical receiver module has 3-dB Bandwidth of 3 GHz. Thus, the single-ended can effectively be applied as a front-end optical Rx in optical interconnect applications.

ACKNOWLEDGMENT

This work was supported by the IT R&D program of MKE/KEIT [10039230, Development of bidirectional 40 Gbps optical link module with low power in Green Data Center for Smart Working Environment] and it was also supported by the Center for Integrated Smart Sensors funded by the Ministry of Education, Science and Technology as Global Frontier Project (CISS-20110031864).

REFERENCES

- [1] T. Takemoto, F. Yuki, H. Yamashita, Y. Lee, T. Saito, "A compact 4 25-Gb/s 3.0 mW/Gb/s CMOS-based optical receiver for board-to-board interconnects", *J. of Lightwave Technology*, vol. 28, no. 23, Dec. 2010, pp. 3343-3350.
- [2] J. Sangirov, I. A. Ukaegbu, T.-W. Lee, M. H. Cho, and H.-H. Park, "Signal Synchronization Using a Flicker Reduction and Denoising Algorithm for Video-Signal Optical Interconnect", *ETRI Journal*, 2012, vol. 34, no. 1, pp. 122-125.
- [3] J. Sangirov, N. T. H. Nguyen, T.-H. Ngo, D.-M. Im, A. I. Ukaegbu, T.-W. Lee, M. H. Cho, and H.-H. Park, "Design of analog-type high-speed SerDes using digital components for optical chip-to-chip link", *Proc. of SPIE*, 2010, vol. 7607 pp. 76071B-1-11.
- [4] J. Sangirov, A. I. Ukaegbu, T.-W. Lee, M. H. Cho, and H.-H. Park, "Low-power and high-speed SerDes with new dynamic latch and flip-flop for optical interconnect in 180 nm CMOS technology", *Proc. of SPIE*, 2011, vol. 7944, pp. 79440V-1-8.
- [5] S. M. Park and C. Toumazou, "A packaged low-noise high-speed regulated cascade transimpedance amplifier using a 0.6μm N-well CMOS technology", *Proc. of 26th European Solid-State Circuits Conference (ESSCIRC)*, 2000, pp. 431 - 434 .
- [6] H. Y. Huang, J. C. Chien, and L. H. Lu, "A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1111-1120, May 2007.
- [7] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18 μm CMOS technology", *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138-2146, Dec. 2003.
- [8] H.-Y. Huang, J.-Ch. Chien, and L.-H. Lu, "A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback", *IEEE J. of Solid State Circuits*, vol. 42, no. 5, MAY 2007, pp. 1111-1120.