Top Down Design of Joint MODEM and CODEC Detection Schemes for DSRC Coded-FSK Systems over High Mobility Fading Channels

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***Abstract*— The joint detection and verification of frequency shift keying (FSK) modulation and demodulation (MODEM), Manchester coding and decoding (CODEC) schemes are proposed for dedicated short range communication (DSRC) systems over high mobility fading channels. The proposed joint coded-FSK detection scheme with low complexity benefit can outperform the conventional separated coded-FSK detection scheme. It is due to the joint scheme with time diversity gain to enhance the detection performance. Moreover, the proposed joint algorithms with floating-point and fixed-point designs are verified in the software-defined-ratio (SDR) platform. Based on the measurement results via SDR equipments, it is confirmed that the implementation of VHDL hardware circuit design of the proposed joint detection scheme can provide robust performance over high mobility Rician multipath fading channel environment.**

***Keywords*— frequency shift keying (FSK) modem, dedicated short range communication (DSRC), coding and decoding (CODEC), software-defined-ratio (SDR).**

I. INTRODUCTION

Recently, the dedicated Short Range communication (DSRC) systems [1]-[2] have drawn a lot of attention for high speed vehicular communications. For the DSRC system, the ASK and FSK modulations with FM0 and Manchester encoders are the mandatory techniques, which can provide for high data rate and high mobility communications. In this paper, we will focus on the FSK modulation and demodulation (MODEM), and Manchester coding and decoding (CODEC) design to enhance the transceiver performance. For the conventional detection scheme, the demodulation and decoding schemes are separated to detect the original transmit signal for DSRC system [3].

However, for the separated receiver, the BER performance would be degraded due to the time-varying fading channel and noise effects. In order to combat the problem, we propose a joint MODEM and CODEC schemes to enhance the detection performance, decrease the energy lose, and reduce the computational complexity. Moreover, we evaluate the BER performance of the floating-point and fixed-point designs for the proposed joint detection schemes. Next, we establish a software-defined-ratio (SDR) platform and measure the experimental result to confirm the feasibility of the above proposed scheme. The SDR platform includes transmitter and receiver equipments, i.e., laptops, WARP FPGA modules [4], WARP DAC/ADC modules, WARP RF Up/Down converter modules, and mobile fading channel equipments. That is, laptops are used to transmit coded-FSK signal which is designed by MATLAB software. Next, the baseband signals are buffered in WARP FPGA module. Then, the analog and RF transmitted signals are generated by WARP DAC and RF Up converter modules. Furthermore, the RF signal is faded by the high mobility channel which is generated by channel emulator. At the receiver, the WARP RF down converter and ADC modules are used to transfer the faded signal back to baseband signal. In the end, the digital signal can be received by laptop via Ethernet cable. Therefore, the MATLAB software can be used to design the joint demodulation and decoding algorithms and detect the original transmitted signal. However, For the DSRC systems, many literatures [5]-[7] are proposed to use SDR techniques to verify or implement the vehicle communications. They are only used for the computer simulation, FPGA module verification, or DSP module evaluation, which are different from the proposed SDR platform. That is, our proposed SDR platform can realize the overall communication system, which involves the real time baseband signal generation, RF up/down converters, mobile fading channel effect, and the received baseband signal processing. To the best of our knowledge, there is no publication paper proposed joint MODEM and CODEC schemes with SDR platform verification for DSRC coded-FSK system.

Finally, based on the above simulation and verification results, the hardware design structure is proposed and implemented by VHDL hardware circuit design. The proposed structure involves the advantage of low computational complexity, i.e. the lower slices and multiplies in implementation. After the implementation of the FPGA hardware modules, it confirms that the proposed algorithms and hardware design structure can be robust realization in the DSRC system over high mobility environments. Summarily, it is noteworthy that the top down design scheme of the proposed system involves with three contributions. Firstly, the joint MODEM and CODEC schemes are proposed to enhance BER performance. Secondly, the SDR platform with

equipments, hardware modules and laptops is established to measure the detection performance of the proposed scheme over high mobility fading channel. Thirdly, a hardware design structure with low computational complexity is proposed and implemented to confirm the proposed detection scheme with robust performance.

II. JOINT MODEM AND CODEC DESIGN FOR DSRC CODED-FSK SYSTEM

Consider a DSRC system over high mobility fading channels. The overall schematic diagram of DSRC coded-FSK transceiver is depicted in Fig. 1.

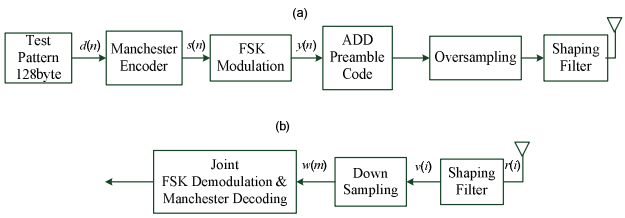

Fig. 1 Transceiver block diagram of the proposed joint MODEM and CODEC design for DSRC coded-FSK systems. (a) Transmitter. (b) Receiver.

At the transmitter, a source data $d(n)$, n=1,…,N is transmitted, where data is consisted of one or zero. Then, using Manchester encoding scheme, they are encoded into s(n) signal. i.e.,

$$\left[s(2n-1) \quad s(2n)\right] = \begin{cases} [0\ 1], & if \quad d(n)=0 \\ [1\ 0], & if \quad d(n)=1 \end{cases} \tag{1}$$

Note that the Manchester encoder generates $s(n)$ signal with $2N$ size. Next, the encoding signal is modulated by FSK modulation scheme [8], i.e.,

$$y(m) = \begin{cases} \cos(2\pi f_1 \dfrac{m}{M}), & if \ s(n)=0 \\ \cos(2\pi f_2 \dfrac{m}{M}), & if \ s(n)=1 \end{cases} \tag{2}$$

The modulation scheme generates two different carrier frequency signals (f_1, f_2) with the duration size being M for each FSK modulation symbol. Thus, the size of the FSK modulated signal of each frame transmission is $2048*M$. As the DSRC system, before the FSK signal is transmitted, a preamble sequence is added to use for the synchronization and channel estimation. Therefore, the overall transmitted signal is expressed by

$$f(k) = \begin{cases} p(k), & for \quad 1 \le k \le K \\ y(k-K), & for \quad K+1 \le k \le K+2048*M \end{cases} \tag{3}$$

where $p(k)$ is the preamble sequence with the size being K and the given sequence being ±1, and $y(k)$ is the FSK modulated signal. Finally, the transmitted signal is up-sampled and convolved by shaping filter, which can generate the band-limited transmitted signal.

$$\begin{aligned} t(i) &= \sum_{i=-\infty}^{\infty} (f(k) \otimes \delta(i-kI)) g_T(i) \\ &= \sum_{i=-\infty}^{\infty} f(k) g_T(i-kI) \end{aligned} \tag{4}$$

where I is the number of oversampling, $\otimes$ is the convolution operation, $\delta(\cdot)$ is the impulse function, $g_T(i)$ is the SRRC filter coefficients with length T. Thus, the modulation and coding signal is transmitted in Fig. 1(a). Moreover, the transmitted signal is up-converted to RF band with 5.8 GHz carrier frequency. Then, it is transmitted through the time-varying multipath fading channel [9]. After the down-convert processing, the digital received signal can be expressed by

$$r(i) = \sum_{l=1}^{L} \alpha_l(i) t(i-\tau_l) e^{j2\pi f_\Delta i} + n(i) \tag{5}$$

where f_Δ is the carrier frequency offset, $n(i)$ is the AWGN noise, L is the number of multipath fading channel, τ_l is the delay time of multipath, $\alpha_l(i)$ is the time-varying fading channel response.

At the receiver, the block diagram is shown in Fig. 1(b). In (5), the transmitted signal is affected by time-varying multipath channel fading and oscillator frequency offset. In order to detect the original transmitted signal, the well-known method is the separated demodulation and decoding schemes. In this paper, we propose a joint demodulation and decoding scheme to detect the original transmitted signal and enhance the detection performance. The receiver design is depicted in Fig. 1(b). First, assume the preamble sequence synchronizing the start time of frame. Thus, the received signal can be designed to match the coefficients of SRRC filter and then down-sample the matched signal, i.e,

$$\begin{aligned} v(i) &= \sum_{j=-\infty}^{\infty} g_T(j) r(i-j) \\ w(m) &= v(mI) \end{aligned} \tag{6}$$

where w(m) is the down-sample received signal after preamble code removal. Next, the down-sampling signal involves the FSK modulation signal and the Manchester coding signal. Therefore, in order to detect the original transmitted signal $\hat{d}(n)$, a joint detection scheme is proposed, i.e., joint FSK demodulator and Manchester decoder :

$$x_1 = \left| \sum_{m=0}^{M-1} w(m) \cos 2\pi f_1 m/M + \sum_{m=0}^{M-1} w(m+M) \cos 2\pi f_2 m/M \right| \tag{7}$$

$$x_2 = \left| \sum_{m=0}^{M-1} w(m) \cos 2\pi f_2 m/M + \sum_{m=0}^{M-1} w(m+M) \cos 2\pi f_1 m/M \right| \tag{8}$$

$$\hat{d}(n) = \begin{cases} 1, & if \quad x_1 < x_2 \\ 0, & if \quad x_1 \ge x_2 \end{cases} \tag{9}$$

In the above equations, x_1 and x_2 are the match filter (MF) output signals for different reference signals consisted by different FSK modulation and Manchester encoding signals. Finally, depending on the MF output energy, we can easily acquire the detect signal. In next simulation and verification section, the floating/fixed point simulation and the SDR platform verification are performed to confirm the proposed joint detection scheme.

III. JOINT MODEM AND CODEC CIRCUIT DESIGN FOR DSRC CODED-FSK SYSTEM

In previous section, the joint MODEM and CODEC algorithms are proposed. Next, we will propose the joint MODEM and CODEC circuit design with low complexity advantage to realize the proposed algorithm. First, the transmitter block diagram is shown in Fig. 1(a). For the hardware design and test, the original data is buffered in ROM with the 128×8 memory size. Then, the source binary data (N=1024) can be acquired by the controller and parallel-to-serial processing of the ROM output data. It is shown in Fig. 2.

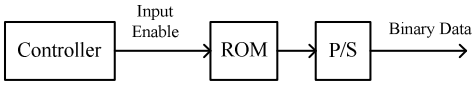

Fig. 2 The block diagram of binary source data generator.

Next, the binary data is encoded by the Manchester encoder in (1), which encoder generates the switching data between (1, 0) and (0, 1). It can be implemented by inverter, multiplexer, and controller, which is shown in Fig. 3. Moreover, the encoded data is mapped for different frequency modulation, i.e., $\cos(2\pi f_1 m/M)$ and $\cos(2\pi f_2 m/M)$. That is, the two ROM memories with single cosine periodic waveform and multiplexing scheme are designed to implement the FSK signals, which are controlled by encoder output data. The implement structure is depicted in Fig. 4. Note that if the coded-FSK modulation scheme is designed by the conventional finite impulse response (FIR) filter, it will induce multiple multiplies to realize the FSK signals. However, for the proposed scheme, we don't use any multiplier which obviously performs the benefit of the low computational complexity.

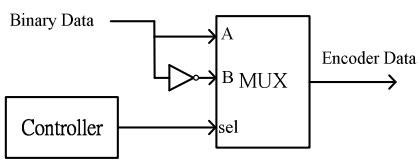

Fig. 3 The circuit design block diagram of Manchester encoder

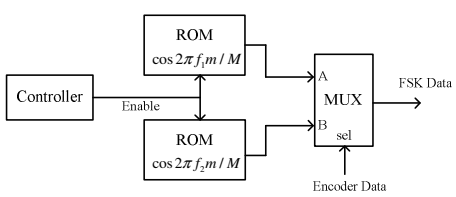

Fig. 4 The circuit design block diagram of FSK modulation.

Next, as shown in Fig. 5, the frame data is constructed by inserting the preamble code into the FSK modulation data. It can be designed by the ROM memory with preamble code, multiplexing, and controller schemes. Finally, at the transmitter, the oversampling and shaping filter schemes need to implement for the band-limited transmitted signal requirement. For the convectional scheme, FIR filter is often used to implement the band-limited signal generation. In this paper, we proposed that the sub-coefficients of filter are selected and outputted by controller, simultaneously. Next, the sub-coefficients are multiplied by the transmitted data with different delay time. Then, using the adder to combine the different delay output data for the band-limited signal transmission, the proposed structure is shown in Fig. 6. It is noteworthy that, for example oversampling size being I=5 and filter coefficient size being T=30, the number of multiplier of the conventional FIR scheme is about 30. However, the proposed scheme only utilizes the 6 multipliers, which is a low complexity design structure. Based on the above design procedures in Figs. 2-6, we can implement the joint FSK modulation and Manchester coding transmission scheme.

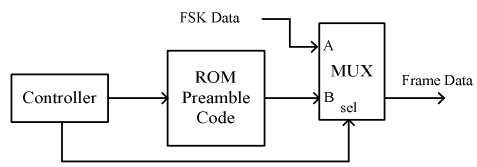

Fig. 5 The circuit design block diagram of Frame data generator

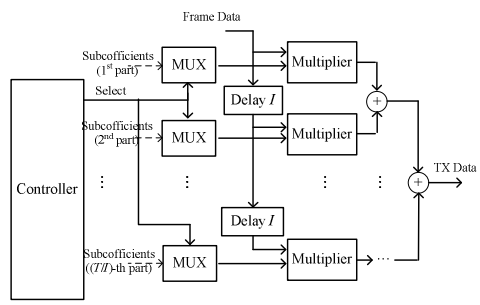

Fig. 6 The circuit design block diagram of over-sampling and shaping filter.

For the receiver side, the block diagram is shown in Fig. 1(b). First, the received signal is filtered by the shaping coefficients and down-sampled to acquire the symbol-based received signal. The received algorithm is described in (6). On the basis of (6), it can be simply implemented by FIR filter. However, the conventional FIR filter design involves multiple multipliers to convolve the received signal, which induces large computational complexity. In order to reduce the computational complexity, we propose the novel filter structure that the filter coefficients with the different delay time are multiplied by the received signal, simultaneously. Next, the multiplied signals are combined by accumulator. Then, the controller and multiplexing schemes are designed to down-sample the parallel output sub-filter data. The proposed design structure is shown in Fig. 7. It obviously reveals that a few multiplier designs can realize the shaping filter and down-sampling schemes.

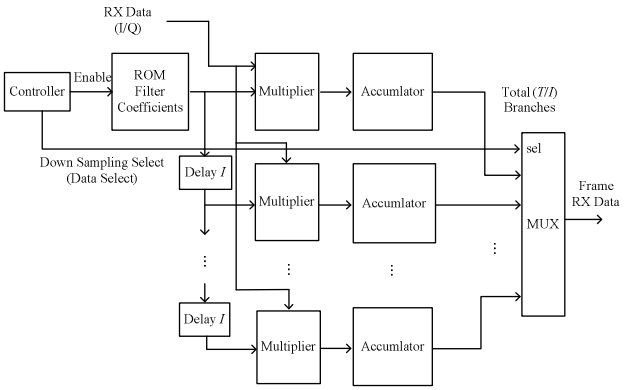

Fig. 7 The circuit design block diagram of down-sampling and shaping filter

Next, as shown in Fig. 1(b), the down-sampled data needs to be demodulated and decoded by the proposed joint processing technique, which the algorithms are proposed in (7)-(9). In order to reduce the computational loading, the two ROM memories with the different frequency shifting waveforms being $2M$ size, i.e., $[\cos(2\pi f_1 m/M)\ \cos(2\pi f_2 m/M)]$ and $[\cos(2\pi f_2 m/M)\ \cos(2\pi f_1 m/M)]$, are used to implement the demodulation and detection schemes of the receiver. That is, using two ROM memories, multiplier, accumulator, I/Q adder, and comparator can implement the joint demodulation and decoding techniques, which is shown in Fig. 8. Note that, the two branches of integrating output data are performed the noncoherent matched filter of FSK signals, which still can be implemented by the conventional FIR filters with larger multipliers. However, for the proposed joint detection design, it can provide low computational complexity advantage.

Overall, the low complexity transceiver design of the joint FSK MODEM and CODEC system is proposed in the implementation section. In next section, the implementation results will confirm the performance of the proposed circuit design structure..

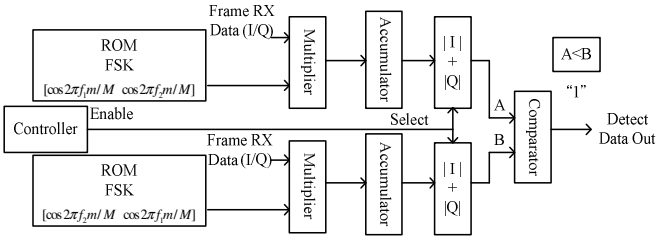

Fig. 8 The circuit design block diagram of joint FSK demodulation and Manchester decoding.

IV. SIMULATION AND IMPLEMENTATION RESULTS

In this section, simulation and implementation results are demonstrated to confirm the performance of the proposed joint MODEM and CODEC transceiver design of the DSRC coded-FSK systems. The simulation parameters of the DSRC coded-FSK systems are summarized in Table 1.

Table 1 Simulation parameters for the DSRC coded-FSK systems.

Simulation Parameters Setting	
Modulation Method	FSK
Encoder Type	Manchester
Packet Data Length	1024 bits
Sinusoidal Frequency Shifting	f_1=1MHz f_2=2MHz
Oversampling Size	5
Shaping Filter Length	30
Multipath Channel Type	2 Path Rician
Velocity of Mobile Fading Channel	100Km/Hr

Next, for all simulations, we assume the ideal frame synchronization. The proposed transceiver performance is evaluated for the floating-point and fixed-point system design over high mobility fading scenarios. Moreover, we establish the SDR platform, which can generate a high mobility Rician fading channel and verify the joint detection algorithm. Finally, VHDL hardware circuit is designed to realize the proposed implementation structure of the joint MODEM and CODEC scheme in Section 3. Then, FPGA platform is used to confirm the hardware design circuit with an efficient implementation and low complexity.

4.1. Computer Simulation

In the first set of simulations, the bit error rate (BER) performance of the proposed joint MODEM and CODEC schemes over time-varying fading channel with mobility 100 Km/Hr is shown in Fig. 9. The simulation results are evaluated by the floating-point design for the proposed system. For the circle line, it is the BER performance of the conventional separated FSK MODEM and Manchester CODEC schemes. The BER performance of the proposed joint scheme is shown in the square line, which obviously provides better performance than the conventional method due to the joint detection being robust to noise and fading channel effects.

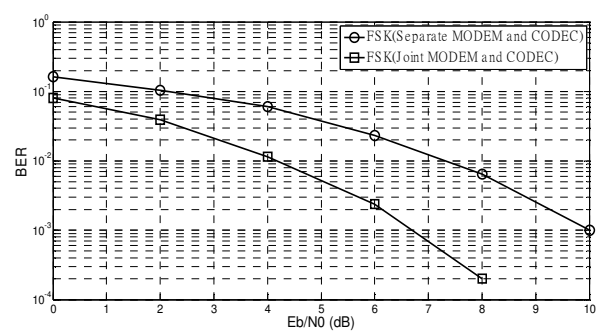

Fig. 9 BER performance as a function of E_b / N_0 for the proposed joint MODEM and CODEC detection scheme, and the conventional separated MODEM and CODEC detection scheme.

In the second set of simulations, we consider the different fixed-point design for the proposed system over high mobility 100 Km/Hr scenario. As shown in Fig. 10, when the number of the fixed-point design is decreased, the BER performance is degraded. Especially, the degradation of the 4 bits fixed-

point design is more serious than other bits. It is because the truncated received signal cannot be efficiently matched by the FSK reference waveforms. For the low complexity and robust performance issues, the 6 bits fixed-point design can be considered for the hardware circuit design to implement the proposed joint detection system.

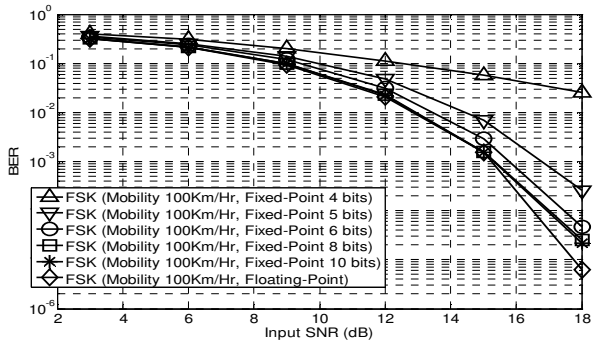

Fig. 10 BER performance as a function of E_b / N_0 for the floating- point and fixed-point design of the proposed joint detection scheme over high mobility fading channels.

4.2. Equipment-Based SDR Platform Verification

To verify the feasibility of the proposed joint MODEM and CODEC detection scheme, SDR platform is established by equipments, radio-board modules, and laptops. The block diagram of the SDR platform with time-varying fading channel emulator is shown in Fig. 11. The SDR platform consists of laptops, WARP FPGA modules, WARP DAC/ADC modules, WARP RF Up/Down modules, and mobile fading channel equipments (Elektrobit Propsim C2 hardware channel emulator [10]).

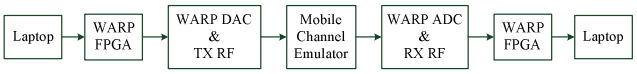

Fig. 11 The block diagram of design structure of SDR platform.

The SDR platform can assist us in verifying the performance of the proposed software algorithms in Section 2. Moreover, the transmitted coded-FSK signal can be generated by the MATLAB program in laptop. Then, the digital signals can be downloaded into WARP FPGA module by Ethernet cable. Next, the analog and RF signals will be up-converted by WARP DAC & RF modules. Thus, the RF signal can be fed into C2 fading channel emulator to perform the mobile fading signal. At receiver side, the WARP RF module down-converts the RF mobile fading signal to the analog baseband signal. Next, the analog signal can be sampled by the WARP ADC module to generate the digital signal. Then, the digital signal can be buffered in the WARP FPGA module and transferred to laptop by Ethernet. Finally, the digital received signal with the joint coded-FSK data via SDR transceiver platform can be synchronized, equalized, detected by the proposed receiver MATLAB software program. Based on the previous SDR design procedures, we can verify the performance of the proposed algorithms in Section 2 over Rician mobile fading channel environment. The overall SDR hardware platform is shown in Fig. 12. Using the SDR platform, the frame error rate (FER) performance results of the floating-point and fixed-point coded-FSK signal detection are shown in Table 2. For the evaluation scenario, the two path mobile Rician fading channel, i.e. 100 Km/Hr, are generated by the C2 channel emulator. Note that, as shown in Table 2, the floating-point and 6 bits fixed-point design can obviously provide better performance than the 4 bits fixed-point design. Moreover, the SDR platform can assist us in confirming the 6 bits fixed-point design for the proposed joint scheme with excellent performance and provide the low computational complexity.

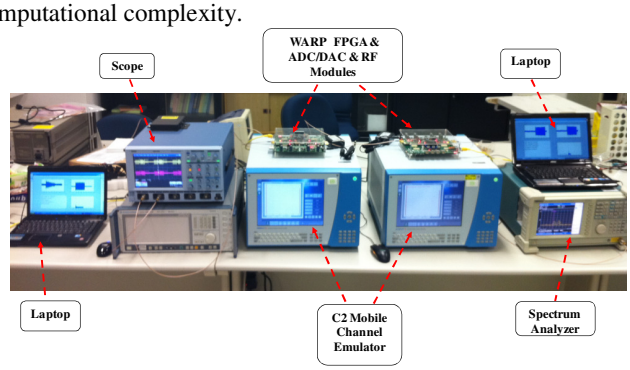

Fig. 12 The hardware prototype of SDR platform.

Table 2 Frame error rate of the proposed joint detection scheme.

FSK Mode		
SNR (dB)	16	18
FER of 4bits Fixed Point	0.342	0.044
FER of 6bits Fixed Point	0.056	0.004
FER of Floating Point	0.048	0.003

4.3. VHDL Hardware Circuit Design and Implement

After the simulation and verification of the above Subsections 4.1 and 4.2, the 6-bits fixed-point design is confirmed for the quantization bit of the hardware circuit implementation of the proposed joint detection scheme. First, on the basis of the hardware structure of the joint MODEM and CODEC schemes in Section 3, we design the VHDL hardware code to realize in Xilinx Spartan 3 FPGA chip, which can operate in 40MHz clock rate.

Based on the FPGA place and route circuit mapping and the component utilization rate in Table 3, it can confirm the transmitter circuit design with low computational complexity, i.e., slices ≈ 2% and multiplies ≈ 30% utilization rate. Moreover, we design the VHDL hardware circuit and implement in Xilinx Spartan 3 FPGA chip for the joint transceiver structure in Section 3. Similar, the circuit mapping result of FPGA place and route in Fig. 13 and utilization rate result of FPGA components in Table 4 still provide lower complexity performance for the overall transceiver design, i.e., slices ≈ 55% and multiplies ≈ 60%. Finally, as shown in Fig. 14, the joint demodulation and decoded data is performed to consist with the original transmitted data, i.e, the golden testing pattern 55, AA, 01, 02, …. Besides, Fig. 14 shows the delay result between the

transmitted data and the received detect data, which is due to the hardware circuit processing delay time. After the above three parts analysis and verification, they confirm that the proposed joint MODEM and CODEC system can provide better performance and lower computation result, which can satisfy the requirement of the DSRC system used for high mobility fading channel environments.

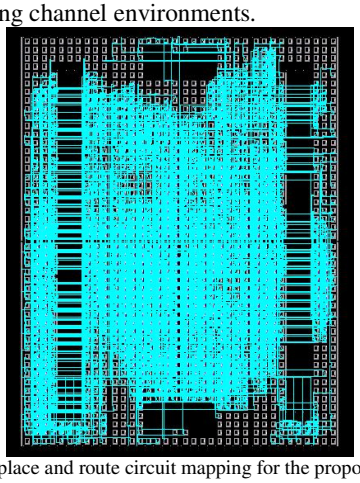

Fig. 13 FPGA place and route circuit mapping for the proposed transceiver VHDL circuit design.

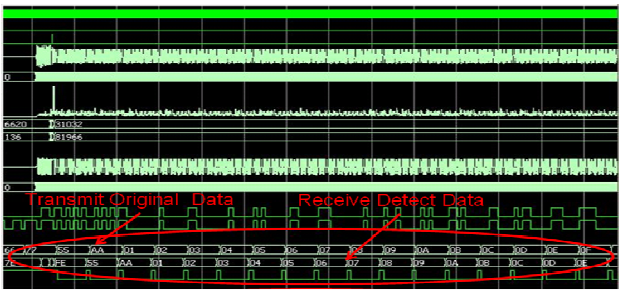

Fig. 14 FPGA implementation result of the proposed VHDL circuit design of the joint MODEM and CODEC scheme.

Table 3 Component utilization rate of the proposed transmitter circuit design in Xilinx Spartan 3 FPGA chip.

Design Summary Report		
Elements	**Utilize Number**	**Utilization Rate**
Slice Flip Flops	215 out of 9312	2%
4 input LUTs	246 out of 9312	2%
MULT18X18SIOs	6 out of 20	30%
bonded IOBs	32 out of 158	20%
Slices	130 out of 4656	2%
BRAMs	2 out of 20	10%
GCLKs	1out of 24	4%

Table 4 Component utilization rate of the proposed transceiver circuit design in Xilinx Spartan 3 FPGA chip.

Design Summary Report		
Elements	**Utilize Number**	**Utilization Rate**
External IOBs	73 out of 158	46%
BUFGMUXs	1 out of 24	4%
MULT18X18SIOs	12 out of 20	60%
RAMB16s	7 out of 20	35%
Slices	2589 out of 4656	55%
SLICEMs	92 out of 2328	3%

V. CONCLUSIONS

The joint detection design and evaluation of the MODEM and CODEC schemes for DSRC coded-FSK system are proposed in this paper. After computer simulation, SDR platform verification, and VHDL hardware design implementation, the proposed system can provide better BER performance and lower computational complexity than the conventional separated detection system. Furthermore, the proposed system can perform the efficiency of the robust detection over high mobility Rician fading channel environments.

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