

A 1.8 V-to-2.5 V MIPI RFFE Slave Interface CMOS Circuit

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Abstract—The MIPI RFFE slave interface circuit including Power-on-Reset (PoR), SCLK receiver and SDATA bi-directional transceiver has been implemented with a CMOS 250 nm process. Simulation results show that the designed circuit has SDATA output transition time (for rise and fall) of shorter than 3.3 ns at a full-speed rate of 26 MHz, which satisfies the timing requirement (< 6.5 ns) by the specification of MIPI RFFE version 1.10. The target load capacitance that the designed MIPI RFFE slave interface circuit drives is 26 pF for the configuration of one master and eight slaves.

Keywords— MIPI, RFFE, master, slave, PoR, SCLK, SDATA, CMOS, driver

I. INTRODUCTION

One of the most crucial features long-term evolution (LTE) communication systems must have is multi-band functionalities [1-3]. This is all because of the frequency fragmentation of LTE with a frequency range from 700 MHz to 2.6 GHz across the world, making mobile phones highly complex with multiple RF front-end devices. To control many different front-end devices such as power amplifiers, switches, filters and antenna tuners, the MIPI Alliance Specification for RF Front-End Control Interface (RFFE) operating with a master/slave configuration has been widely used for that purpose [4]. The MIPI RFFE slave consists of mainly two blocks: digital logic for the slave operation and analog interface circuits for the slave logic to interface with its master in an RFFE configuration. In comparison with the RFFE slave logic, however, an interface circuit is not well defined but only described in a functional level because the interface circuits is dependent on a process on which MIPI RFFE slave logic is implemented.

In this paper, a 1.8 V-to-2.5 V MIPI RFFE slave interface CMOS circuit on a 250 nm CMOS process is designed and its results are described in detail to provide one of the possible MIPI RFFE slave interface circuits. The voltage level of the pair of master and slave is 1.8 V (by MIPI RFFE IO level specification) and the slave logic has been implemented with 2.5 V CMOS devices.

The remainder of this paper is organized as follows. In Section II, the overall architecture of the designed MIPI RFFE slave circuit is described; in Section III, the design results of circuits of Power-on-Reset (PoR), SCLK receiver and

SDATA bi-directional transceiver are discussed respectively; and the summary of the paper is given in Section IV.

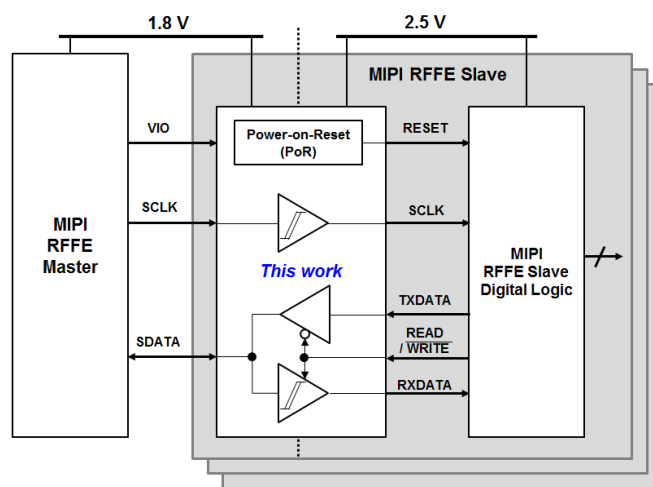


Figure 1. The designed MIPI RFFE interface block diagram

II. DESIGNED RFFE INTERFACE

The overall structure of a designed MIPI RFFE interface in a configuration of a master with multiple slaves is shown in Fig.1. With the single RFFE control interface, multiple slaves in RF front-end devices such as power amplifiers, low-noise amplifiers, switches and antenna tuners can be controlled by the master, providing a simple and powerful control solution for RF front-end devices. The emphasis of the paper is on the design of the MIPI RFFE slave interface circuits including PoR, SCLK receiver and SDATA bi-directional transceiver, which enables digital bits generated from the master to be transmitted to the slave digital logic through the single control bus and vice versa. The PoR circuit provides reset signal, active low in our design, to the slave digital logic at the beginning when the power of the RFFE slave is on. With the reset signal, the slave digital logic is initialized and prepared to communicate with its RFFE master. To transmit and receive digital control bits between a master and a slave, SDATA bi-directional transceiver is used with a READ/WRITE bit. For synchronization, a clock signal is provided from the master to the slave through SCLK line with

a SCLK receiver. Typically, for a more reliable digital signal acquisition performance, receivers in SCLK and SDATA adopt Schmitt -trigger-based comparator.

III. CIRCUIT DESIGN

The MIPI RFFE slave interface circuit including PoR, SCLK receiver and SDATA bi-directional transceiver has been implemented with a CMOS 250 nm process. All transistors used in the circuit are 2.5 V MOSFETs.

A. Power-on-Reset (PoR)

The designed PoR circuit is composed of three blocks: cascaded current mirrors with a current generator, a MOS-based delay cell and a RESET pulse generator based on a Schmitt trigger [5].

When a 2.5 V supply voltage is applied to the PoR circuit, a $3\mu\text{A}$ current starts to flow through M9, M10 and M11. The current is then copied by M8, M7, M6, M5 and M1 and only 3 nA current is injected into the delay cell, increasing the gate potential of M9 at a very slow rate due to the extremely small amount of the current ($= 3\text{ nA}$). To obtain even longer delay at the RESET pulse generator output, a Schmitt trigger is used and then the RESET output pulse (active low) at the inverter is toggled not at the middle level of the supply, 1.25 V, but at the level higher than the half supply level.

The transient simulation results of the designed PoR circuit are shown in Fig. 3. As shown in the figure, when the 2.5 V signal is applied to the supply of the PoR circuit, the gate potential of the delay cell of M9 starts to increase slowly. The output signal of the Schmitt trigger is toggled from 0 V to 2.5 V at a threshold level of about 1.85 V [6].

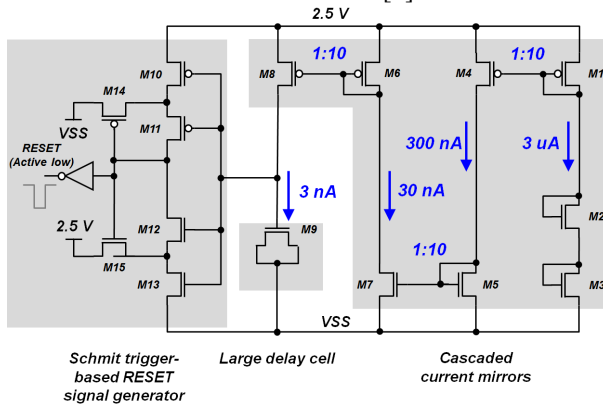


Figure 2. Circuit diagram of the designed PoR

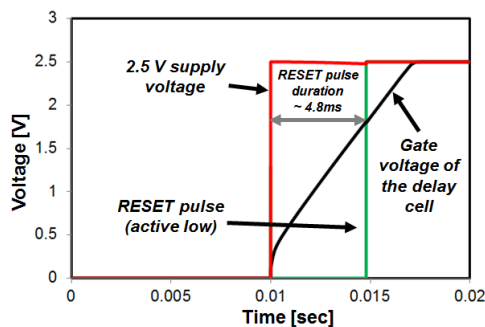


Figure 3. Simulated transient waveforms of several nodes of the designed PoR circuit

B. SCLK Receiver

Since the interface voltage level of MIPI RFFE is 1.8 V and the logic signal level of the used process is 2.5 V, a 1.8 V-to-2.5 V level shifting function must be implemented in the MIPI RFFE slave interface circuit for the two different voltage levels. The circuit diagram of the designed SCLK receiver is shown Fig.4. To obtain a clean clock signal from a SCLK signal generated by a RFFE master, hysteretic differential comparator is used. Also, it does level converting operation (1.8 V to 2.5 V). The two resistors of R1 and R2 help M5 and M6 easily toggle their output signal, even with a low-level input signal, by lowering the drain voltages of the FETs due to voltage drops through the resistors.

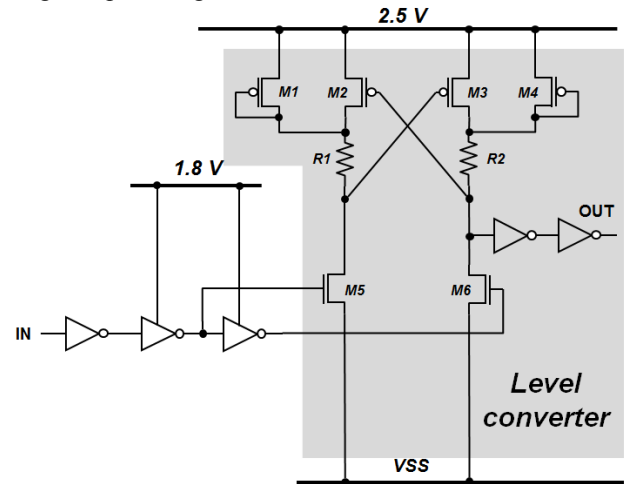


Figure 4. A circuit diagram of the design SCLK receiver

C. SDATA Bi-directional Transceiver

One of the main advantages of MIPI RFFE against other competitors is that it requires only two signal lines for data communication. One is for clock and the other one is bi-directional data. Therefore, for SDATA, bi-directional transceivers are adopted not only in a master but also in a slave.

Fig. 5 shows a block diagram and circuits of SDATA bi-directional transceiver.

In the TXDATA path, a 2.5 V-to-1.8 V level converting operation is done by a simple cascaded inverter chain with different power supplies. This is because the output level of 1.8 V is lower than the input 2.5 V level, making the transistors in the inverter with a 1.8 V supply fully switched on and off by the higher input driving signal level. According to the MIPI RFFE specification, the total capacitance of a SDATA node with an eight-slave-configured RFFE bus interface is 26 pF [4]. Thus, the transistor size of the output buffer, tri-state inverter in Fig. 5, is chosen so as to drive the highly capacitive load and to satisfy the timing requirement by the RFFE specification. According to the specification, SDATA output transition (rise/fall) time is in the range from

2.1 ns to 6.5 ns at a full speed rate of 26 MHz [4]. Transient waveform simulation results of the SDATA transmitter are shown in Fig. 6(a). The simulated propagation delay of the SDATA transmitter is 1.9 ns. The rise and fall time of the SDATA transmitter output signal are 3.3 ns and 3.0 ns, respectively, which is definitely within the transition time range of 2.1 ns to 6.5 ns, satisfying the timing requirement of MIPI RFFE.

In the RXDATA path, a tri-state buffer is designed and used at the input of the SDATA receiver so that the receiver is not affected by the transmitted data signal when a READ signal is OFF. Only when the READ signal is ON, the SDATA signal is transferred to the level converter in the receiver through the tri-state buffer and received by a RFFE slave digital logic circuit. In fig. 6(b), the simulated waveforms of SDATA and RXDATA of the designed SDATA receiver are shown. The propagation delay between SDATA and RXDATA signals is 0.8 ns.

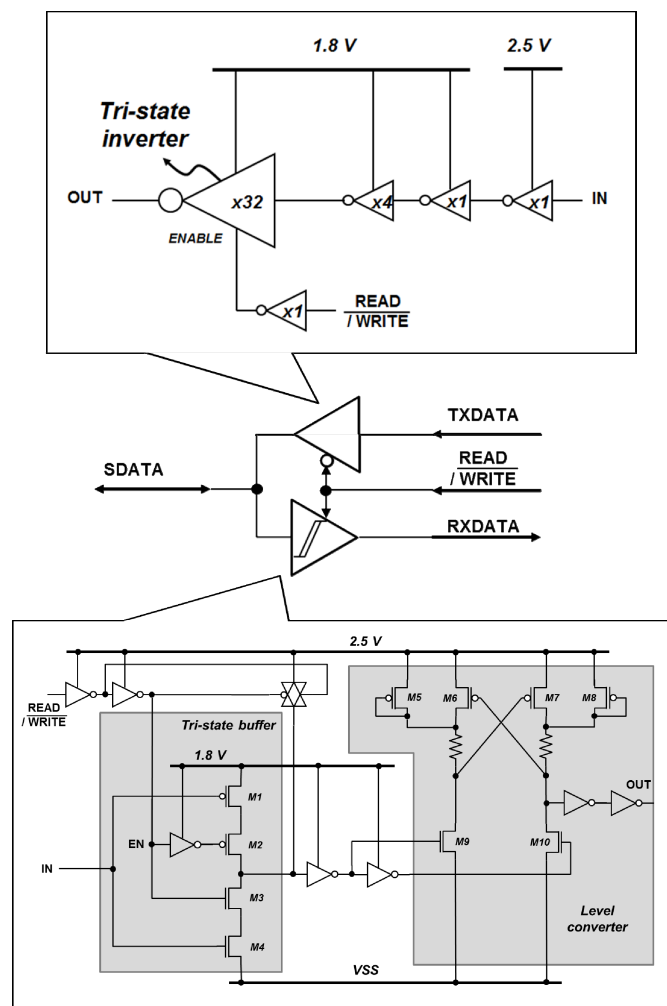
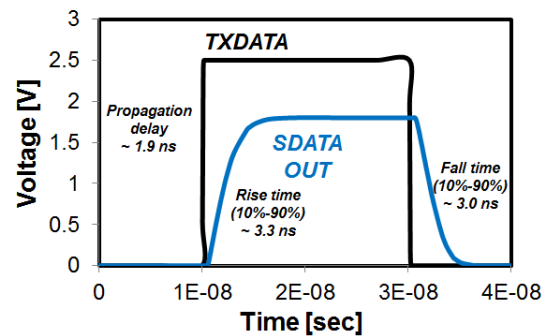


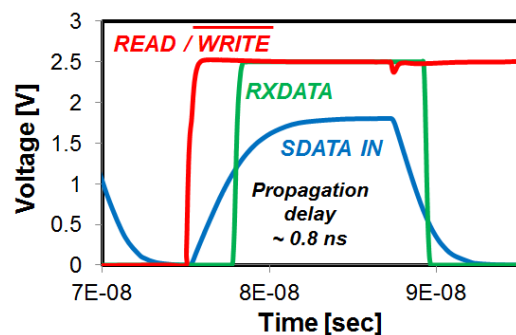
Figure 5. Block diagram and circuits of SDATA bi-directional transceiver

D. Implemented MIPI RFFE Slave Interface Circuit

Fig. 7 shows the layout of the designed MIPI RFFE slave circuit including a PoR, a SCLK receiver, a SDATA bi-directional transceiver and a slave digital logic. The size of the slave block is 370 μ m x 510 μ m on a standard CMOS 250 nm process.



(a)



(b)

Figure 6. Simulated transient waveforms of the designed SDATA bi-directional transceiver: (a)SDATA transmitter waveforms and (b)SDATA receiver waveforms

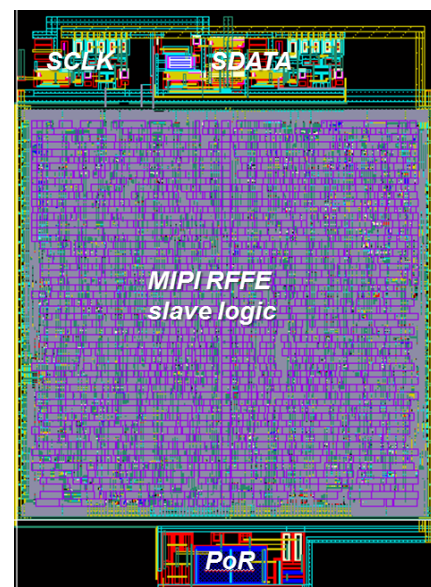


Figure 7. The layout of the designed MIPI RFFE slave interface circuit with a slave digital logic circuit

IV. CONCLUSIONS

In this paper, a 1.8 V-to-2.5 V MIPI RFFE slave interface CMOS circuit in compliance with the MIPI RFFE specification version 1.1 is designed. The interface circuit includes PoR, SCLK receiver and SDATA bi-directional transceiver. The output transition time for rise and fall is shorter than 3.3 ns at a 26 MHz full-speed rate with a 26 pF load capacitor for the possible configuration of a master and up to eight slaves. The size of the designed chip including the interface circuits and a slave digital logic was 370 μ m x 510 μ m on a 250 nm CMOS process.

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