

MEMS Switch as High Speed Sample and Hold Circuit

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Abstract–This paper introduces a use of special design MEMS used as low insertion loss sample and hold (S/H) circuit, replacing the GaAsFET switch with MEMS switch. The use of electrostatic MEMS switches is attractive because of its advantages, such as very low power consumption ,low insertion loss and high isolation. The introduced MEMS switch is capable to perform at high speed, since it does not include transistor in its structure. insertion loss in the case of GaAsFET switch is -10.506 dB while its value in the case of MEMS switch is -.086 db at 20GHZ, the proposed circuit have insertion loss reduction 99.2% .

I-INTRODUCTION

With the increasing demand for high quantization capability and high sampling rate in data acquisition systems, the performance of the S/H circuits is becoming more and more important . This is especially true since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their sampling rate is low with high insertion loss. S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits [1-4]. As a result, better and faster S/H circuits must be developed. At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor. However, due to the limitations of the FET transistor switches, errors due to charge injection and clock feedthrough restrict the performance of S/H circuits. As a result, The use of electrostatic MEMS switches is useful because of its advantages, such as high isolation. However, Many previous researches focus on RF MEMS switch, which presents a good performance at microwave frequency. This results in an increasing use of RF MEMS switches for telecommunication purposes in the last ten years [5-10].

II- Basics and Performance of S/H circuits

A simple S/H circuit consists of a switch and a capacitor [Fig. 1 (a)]. A FET transistor can serve as a switch [Fig. 1(b)] because (a) it can be on while carrying zero current, and (b) its source and drain voltages are not “pinned” to the gate voltage, i.e., if the gate voltage varies, the source or drain voltages need not follow that variation. By

contrast, bipolar transistors lack both of these properties, typically necessitating complex circuits to perform S/H.

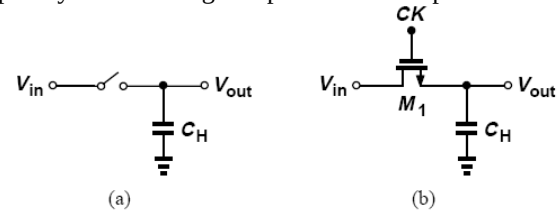


Fig. 1 (a):Schematic S/H circuit, (b) implementation using FET switch Transistor.

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs). The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Fig. 1, where V_{in} is the input signal, M_1 is an MOS transistor operating as the sampling switch, C_H is the hold capacitor, ck is the clock signal, and V_{out} is the resulting S/H output signal.

When the switch is closed, the capacitor C_H is charged to the value of the input voltage V_{in} , the sample stage. Afterwards the switch is opened and the capacitor retains its charge, the hold stage.

The resulting output is shown in Fig.2. This alternation between S/H modes is repeated as long as the switch keeps toggling. The switching rate is controlled by a clock signal whose frequency should satisfy the sampling criterion.

The beat test method is popular. In this test, the S&H circuit operates at its maximum clock frequency and apply a sinusoidal input signal that has a frequency slightly different than the clock frequency. The output is then demodulated to a low frequency equal to the difference between the frequency of the clock signal and that of the input signal, which is then analyzed using a spectrum analyzer or using FFT in computer.[1]

To fully characterize an S/H circuit, specifications of characteristic parameter both in the time domain and in the frequency domain have to be defined as follows:

The **acquisition time** is the time from the command to switch from hold mode to sample mode to the moment when the circuit is ready to take a new sample, i.e. it

tracks the input. Acquisition time is one of the parameters that define the maximum achievable sampling rate.

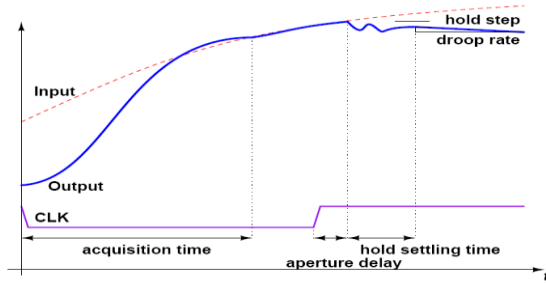


Fig. 2: Time domain S/H circuit performance. [11]

The **aperture time** or **aperture delay** is the fixed time from the sampling command to the moment when the sample is actually taken. Random variation in the sampling moment is known as **aperture uncertainty** or **aperture jitter**. The **hold mode settling time** determines the time from the sampling moment to the moment when the circuit output has settled within the specified accuracy of its steady state value. If the S/H circuit is used in front of an ADC, the ADC can digitize the S/H circuit output at that moment. The hold mode settling time has a major impact on the maximum sampling rate of the S/H circuit. The signal may leak from the circuit when in hold mode. The rate of change in output that results from this is specified by **the droop rate**.

In hold mode an S/H circuit remembers the value of the input signal at the sampling moment, and thus it can be considered as an analog memory cell. The basic circuit elements that can be employed as a memory are capacitors and inductors, of which the capacitors store the signal as a voltage (or charge) and the inductors as a current. In addition to the inductor, a current memory needs a switch that is a good short circuit when it is closed. Similarly, a switch which is a good open circuit in its off-state is needed for a voltage memory. Since capacitors and switches with a high off-resistance are far easier to implement in a practical integrated circuit (IC) technology than inductors and switches with a very small on-resistance, all sample-and-hold circuits are based on voltage sampling. There also exists current mode S/H circuits, but they always include voltage-to-current and current-to-voltage converters which allow the sampled quantity to be voltage.[1]

III-Charge Injection

A conducting MOS switch has a finite amount of mobile charge in its channel. When the transistor is turned off, this charge is distributed between the source, drain, and bulk terminals of the device. To design accurate Switched Capacitor (SC) circuits the nature of this charge injection and redistribution phenomenon must be understood. Through the years the charge injection has been analyzed and discussed in various papers [12-14]. In real circuit the resistance of the MOS switch cannot be changed from its constant on-value (the nonlinear effects

are neglected in this discussion) in tracking mode to infinite in zero time. This is due to the finite slope of the transistor gate voltage and the gate voltage feedthrough to the source and drain via the parasitic capacitances. Since there is no single time instant which can be said to be the sampling moment, the sampling must be modeled with the sampling function.[1]

A thorough analysis of the nMOS transistor sampling function based both on analytic formulation and simulations is presented in [14]. The authors define the aperture time as the time interval which covers 80% of the sampling function area. Their analysis shows that for very small sampling capacitor values the aperture time has an almost linear dependence on the gate voltage fall time. On the other hand, when the sampling capacitor is large, the sampling function is dominated by the tracking mode time constant, which is typically the case in S/H circuits. Sub-samplers and digital high-speed line receivers are applications where the bandwidth reduction resulting from the finite turn-off time is remarkable.

An ideal S/H circuit takes samples of an input signal at uniform intervals T . In the time domain this corresponds to multiplying the signal by an impulse train

$$y(t) = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT) \quad (1)$$

where $\delta(t)$ represents Dirac's delta function. The result is a train of impulses whose values correspond to the instantaneous values of the input signal.

The time domain representation of a S/H signal is a convolution of the sampled signal (1) and a square pulse

$$y(t) = \left[x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT) \right] \star \Pi\left(\frac{t}{T} - \frac{1}{2}\right) \quad (2)$$

where $\Pi(t/T - 1/2)$ denotes a square pulse from $t = 0$ to $t = T$. In the frequency domain the convolution corresponds to multiplication and thus the spectrum of the sampled-and-held signal is the spectrum of a sampled signal multiplied by the spectrum of the square pulse, which has the form of $\sin(x)/x$. [1]

IV. PROBLEM DEFINITION

Fig.3 shows the schematic of the basic NMOS sample and hold circuit. Line diagram ADS have used for simulation for results, The NMOS FET used. Fig.4 shows a timing diagram for the pulse f that applies to the gate of transistor .

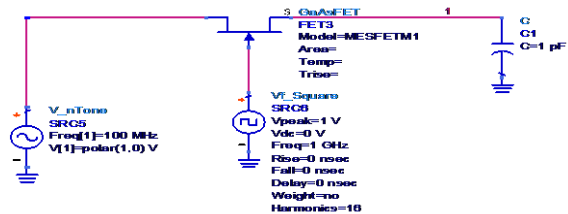


Fig. 3: implementation of the switch by a FET transistor when the clock f at the gate of the FET goes high (V_{DD}), the switch is switched on and capacitor C_H is shorted to the input. In this case NMOS is in sampling mode,

that $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$. The gate to source voltage is given by

$$V_{GS}=V_G-V_S \quad (3)$$

$$V_{GS}=V_{DD}-V_{in} \quad (4)$$

V_{GS} gate-source voltage, V_{th} threshold voltage

From equations 4 it is seen that when apply V_{DD} at the gate of transistor then V_{GS} will depend on V_{in} . In order to remove the effect of clock, voltage should be equal to $(V_{DD}+V_{in})$

This will make V_{GS} independent of V_{in} . When the input becomes low (zero), the switch goes into off mode. This results in the input voltage value being held on the hold capacitor. Thus in this case NMOS is in the hold mode.

The NMOS has used for the design of S/H circuit instead of PMOS because :

- Electrons, which are carriers in an n-channel device, are about two times as mobile as holes, the carriers in a p-channel device. An n-channel device is therefore faster than a p-channel device.
- Since electron mobility is almost twice that of a hole, the on of an n-channel device will be half that of an equivalent PMOS device operating under same conditions with the same. Thus n-channel transistors that are only half the size of p-channel devices will have the same impedance. Therefore, complex n-channel ICs can be implemented without any increase in area of silicon.
- N-channel circuits have a speed advantage over PMOS as the junction areas are smaller. Considering the fact that the speed of the operation of an MOS IC is significantly reduced by internal RC time constants, and also the capacitance of the diode is proportional to diode size, an n-channel junction might have smaller capacitance. This, in turn, enhances its speed.

While the circuit in Fig.3 has the advantage of being simple in construction, it also has a few disadvantages. When switch S is turned off, some of the channel charge of the NMOS transistor gets heaped on to the hold capacitor. As this charge depends on the signal and is nonlinear, this will cause distortion in the output voltage of the hold capacitor C_H . Plus, the exact sampling instant is dependent on the gate-source voltage V_{gs} of the switch and transistor threshold voltage V_{th} . [12-16]

IV. MEMS Switches

MEMS refer to a 21st century technology named micro-electromechanical systems. MEMS are processes technology used to create tiny integrated devices or systems that combine mechanical, electrical and electronic components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimeters. These device systems have the ability to sense, control, actuate and generate on the macro scale. In the most general form, MEMS consist of mechanical microstructures, micro-sensors, micro-actuators and microelectronics, all integrated onto the same silicon chip. Nowadays, MEMS have a diversity of applications

across multiple markets like automotive, electronics, medical, communications, and defense weapons. MEMS switches are surface-micro machined devices which use a mechanical movement to achieve a short circuit or an open circuit in the RF transmission-line. RF MEMS switches are the specific micromechanical switches which are designed to operate for m 0.1 to 100 GHz [7-9]. With the recent exciting advancements in the field of miniaturized MEMS switch have shown to offer a superior RF performance in comparison to their semiconductor counterparts. [10,17-19]

IV. The PROPOSED MEMS S/H

In Fig.4 an MEMS switch is replaced instead of GaAsFET Switch, that has a number of benefits. The channel charge and resistance are not found on the input voltage V_{in} , implying that distortion can be minimized., it results in a fast and low power circuit.

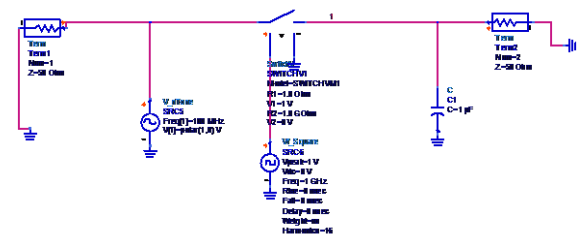


Fig. 4: implementation of the proposed MEMS switch.

The proposed circuit components are:

- Clock Freq. =1 GHz
wave form =square wave
voltage amplitude =1V
- Input signal Freq.=100, 600, 900 MHz
wave form = sin wave
voltage amplitude =1V

as illustrated in Fig.5

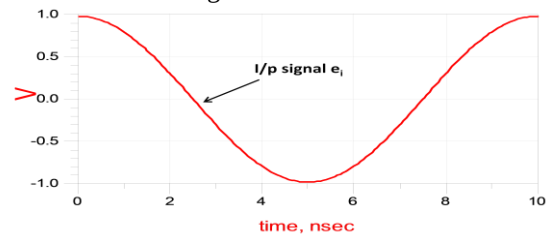


Fig. 5:The Input signal amplitude 1V, Frequency100 MHz.

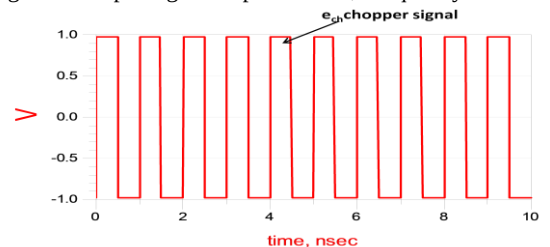


Fig. 6:The chopper signal amplitude 1V, Frequency1 GHz.

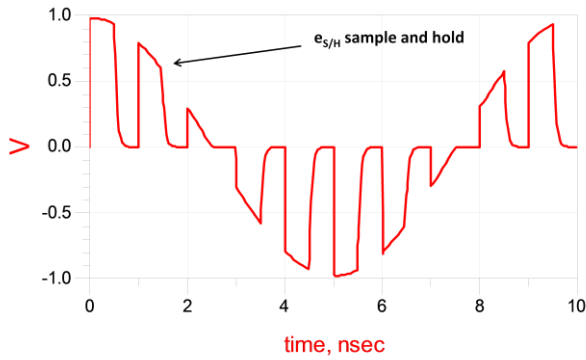


Fig. 7: The output S / H signal using MEMS switch

V. RESULTUS

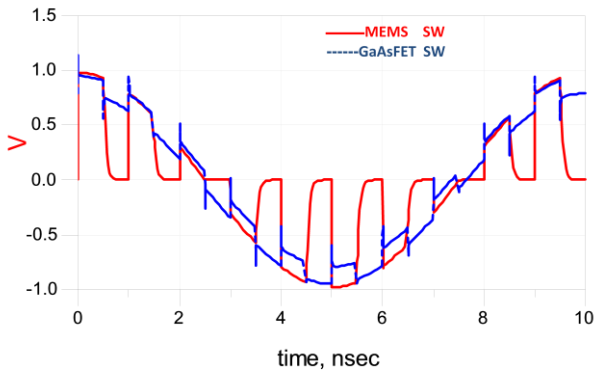


Fig. 8: Timing diagram of GaAsFET switch vs MEMS switch.

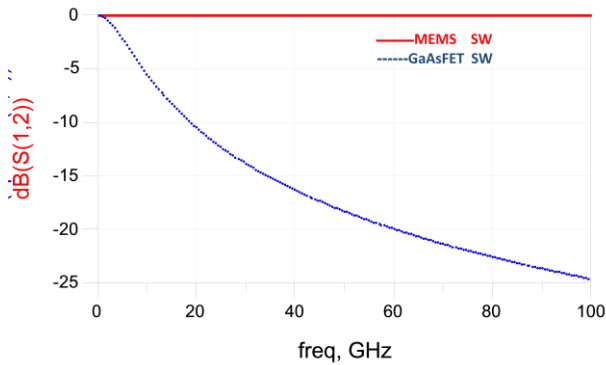


Fig. 9: insertion loss of GaAsFET switch vs MEMS switch.

It can be notice that , insertion loss in the case of GaAsFET switch is -10.506 dB while its value in the case of MEMS switch is -.086 db at 20GHz thus the

Table (1)insertion loss for GaAsFET switch vs MEMS switch

Freq(GHz)	0.5 GHz	1GHz	10GHz	20GHz
Devises				
GaAsFET (dB)	-0.114	-0.193	-5.505	-10.506
MEMS (dB)	-0.086	0.086	-0.086	-0.086
Δ dB	0.028	0.107	5.419	10.42
Reduction%	24.56%	55.4%	98.4%	99.2%

where
$$\text{Reduction\%} = \frac{FET - MEMS}{FET} * 100$$

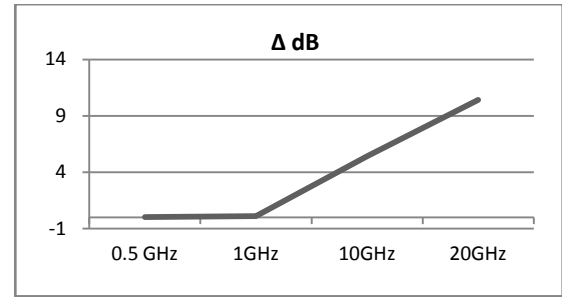


Fig. 10: The deference in insertion loss using MEMS

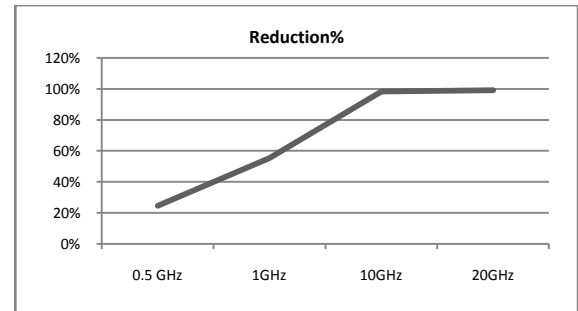


Fig. 11: The Reduction in insertion loss using MEMS

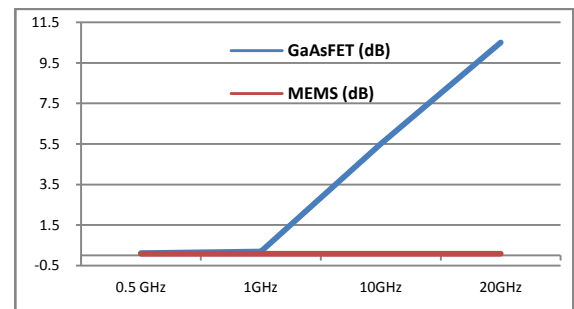


Fig. 11: insertion loss of GaAsFET switch vs MEMS switch

MEMS switch provides low insertion loss (< 0.1dB) FET switches have higher insertion loss performance at higher frequencies due to the higher ON resistance of FETs

VII. CONCLUSION

The proposal introduced in this paper can perform much smoother sample and hold operation. Power consumption is minimized as operational amplifier is not used. Another benefit is low insertion loss MEMS switch provides low insertion loss (<0.1dB), which again minimizes distortion. Additionally, this circuit does not have a problem with Charge Injection.

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BIOGRAPHIES



Mazhar B. Tayel was born in Alexandria, Egypt on Nov. 20th, 1939. He was graduated from Alexandria University Faculty of Engineering Electrical and Electronics department class 1963.

He published many papers and books in electronics, biomedical, and measurements. Prof. Dr. Mazhar Basyouni Tayel had his B.Sc. with honor degree in 1963, and then he had his Ph.D. Electro-physics degree in 1970. He had this Prof. degree of elect. and communication and Biomedical Engineering and systems in 1980. Now he is Emeritus Professor since 1999. From 1987 to 1991 he worked as a chairman, communication engineering section, EED BAU-Lebanon and from 1991 to 1995 he worked as Chairman, Communication Engineering Section, EED Alexandria. University, Alexandria Egypt, and from 1995 to 1996 he worked as a chairman, EED, Faculty of Engineering, BAU-Lebanon, and from 1996 to 1997 he worked as the dean, Faculty of Engineering, BAU - Lebanon, and from 1999 to 2009 he worked as a senior prof., Faculty of Engineering, Alexandria. University, Alexandria Egypt, finally from 2009 to now he worked as Emeritus Professor, Faculty of Engineering, Alexandria University, Alexandria Egypt. Prof. Dr. Tayel worked as a general consultant in many companies and factories also he is Member in supreme consul of Egypt. E.Prof. Mazhar Basyouni Tayel.



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