

A NOVEL MEMS CHARGE-PUMP CIRCUIT

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Abstract—This paper presents a novel MEMS charge-pump circuit design and simulation for PLL applications. The proposed circuit increases switching speed, minimizes power consumption and reduces the static Charge and Charge injection cancellation. The Advanced Design System (ADS), from Agilent Technologies are used in the proposed structure for high frequency applications. The use of electrostatic MEMS switches is attractive because of its advantages, such as very low power consumption, low insertion loss and high isolation. This paper introduces a use of special design MEMS as a charge pump circuit, replacing the GaAs FET switch with MEMS switch. The proposed charge pump circuit can generate higher output voltage with 66.3% improvement when compared with the charge pump using MOS devices

Keywords— MEMS, PLL, charge-pump, GaAs FET switch, MEMS switch

I-INTRODUCTION

The phase-locked loop (PLL) is a feedback loop in which oscillator is set to match the phase of a given reference signal. When the two signals are locked in phase they will also be locked in frequency. The output signal from the PLL will thus be an electrical signal oscillating at a relative reference frequency. Various applications of the PLLs are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizers in communication systems for clock extraction [1,2].

A basic form of a PLL consists of five blocks namely:

1. Phase frequency Detector (PFD)
2. Charge Pump (CP)
3. Loop Filter (LF)
4. Voltage Controlled Oscillator (VCO)
5. Frequency divider (1/N)

Due to continuous power supply reduction, charge pump circuits are widely used in integrated circuits (ICs) devoted to several kind of applications, such as smart power, non-volatile memories, switched capacitor circuits, operational amplifiers, voltage regulators, SRAMs, LCD drivers, piezoelectric actuators, RF antenna switch controllers, etc. [1]

II-Phase Locked Loop

A schematic diagram of a basic PLL circuit is shown in Figure 1. The input is given from a reference frequency signal source. The phase detector compares the voltage controlled oscillator (VCO) output signal frequency to the reference signal frequency and generates a DC voltage proportional to their phase differences. This

voltage is then fed through a charge pump and low-pass loop filter to the VCO. The VCO output is then fed back the frequency divider (1/N) to the phase detector. This results in a feedback loop, where the voltage controlled oscillator will be tuned to match the phase (and frequency) of the input reference signal.[1-4]

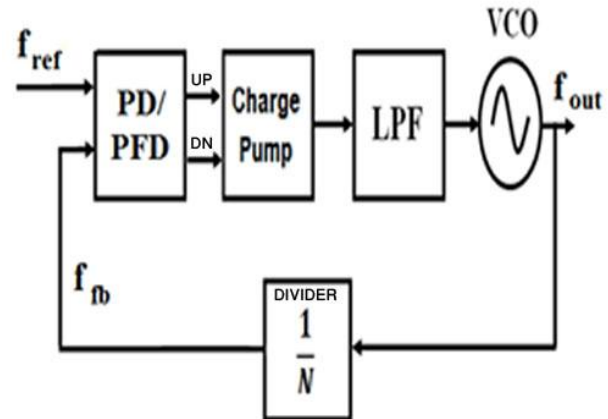


Fig. 1 : Basic block diagram of an PLL [1].

A-Phase-Frequency detector (PFD)

The phase-frequency detector (PFD) is a more advanced version of a component known as the phase detector (PD). A phase detector is an electronic block which compares the phase difference between the two input signals and then gives an output signal that is proportional to phase difference, in accordance with

$$v_{out} = K_d (\Theta_{ref} - \Theta_{VCO}) \quad (1)$$

where v_{out} is the output voltage, K_d is the phase detector's gain, Θ_{ref} is the phase of the reference signal and Θ_{VCO} is the phase of the VCO's output signal. Thus a large phase difference will give rise to a large output voltage. It will however wrap around at large phase differences depending on the type of phase detector used[5-6]

B-Loop filter

The output voltage from the passive LPF is the control voltage of VCO which increase/decrease frequency in such a manner that, the voltage output is maintained proportional to the charge of the capacitor [1,4].

C-Voltage Controlled Oscillator (VCO)

This is the most important block of PLL system that helps to produce output frequency according to voltage.

The VCO is fully differential based ring oscillator consisting of three parts : voltage to current converter, current controlled oscillator (CCO) and level shifter, The voltage to current converter converts the input voltage into a biasing current for the current controlled oscillator (CCO), which features an oscillation frequency proportional to the biasing current. The level shifter converts the small amplitude CCO output signal into a rail to rail CMOS level signal[1,2].

D- Frequency Divider

For clock generation, mostly reference frequencies are limited by the maximum frequency decided by a crystal frequency reference, The divider's purpose is to scale down the frequency from the output of the voltage controlled oscillator so that the system can operate at a higher frequency than the reference signal thus the VCO has to be designed such that the output of VCO is = N times the reference frequency. So the output of the VCO is passed through a divide by N-counter and feedback to the input.[1,4]

II- Charge Pump

The Charge Pump (CP) is the next block after the PFD. The outputs *up* and *down* signals of the PFD are connected directly to CP. Basic CP converts logic states of the PFD output into analog signal making it suitable to control VCO frequency. In modern PLL design, the CP is usually paired with PFD due to its wide locking range and low cost. The function of CP is to inject a constant amount of DC voltage into the loop filter [7-8]. A simple CP consists of two switched CMOS sources that pump charge into or out of the loop filter according to the PFD outputs. Fig. 2 shows a simple charge pump driven by a PFD and driving a capacitor load

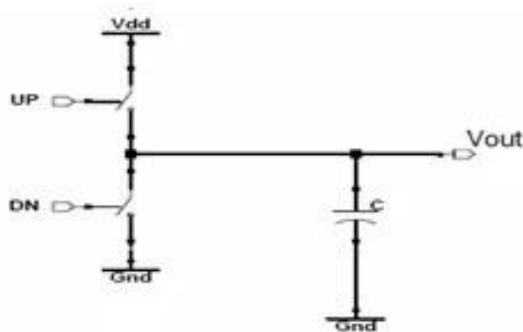


Fig. 2 : simple systematic charge pump [2]

The timing diagram operation of the CP is shown in Fig. 3. The two switches of the CP are controlled by the UP and DN signals from the PFD. When UP is high and DN is low, the voltage source of the CP is active and sources the voltage V_{DD} into the load. When UP is low and DN is high, the voltage sink is active and voltage sinks into the load. When UP and DN are either both high or both low, there isn't any net voltage flow to or from the load. In

this way, the output voltage of the CP is proportional to the pulse width difference of UP and DN signals, which is the phase difference of the two inputs to PFD. A good charge pump should feature equal charge and discharge voltage, minimum switching errors such as charge injection, charge sharing, and clock feedthrough, and minimum output voltage mismatches.

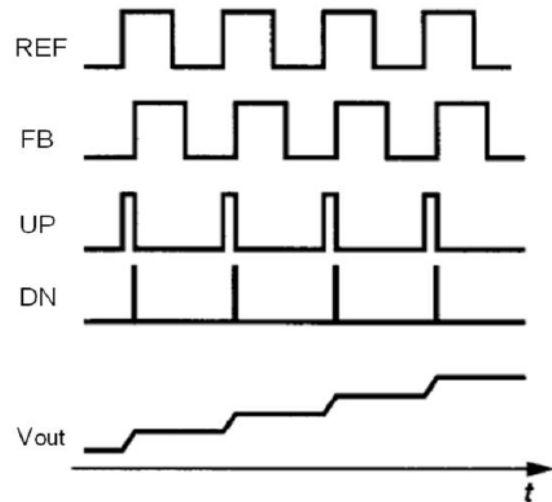


Fig. 3 : Output voltage waveform of the LF when UP signal is activated [1-2]

Table (1) PFD Logic State

UP	DN	Output
0	0	No change
1	0	Charge
0	1	Discharge
1	1	No change

Table (1) shows charge pump input which charges and discharges LF according to output from PFD

IV. PROBLEM DEFINITION

Fig.4 shows the schematic diagram of the basic CP circuit. Line diagram ADS have used for simulation for results. However, the resulting circuit performance is limited due to the threshold voltage drop of the MOS devices and the reverse charge-sharing phenomenon. Moreover, for high output generated voltages, the increase in the threshold voltage due to the body effect, can significantly reduce the pumping gain.[7-9]

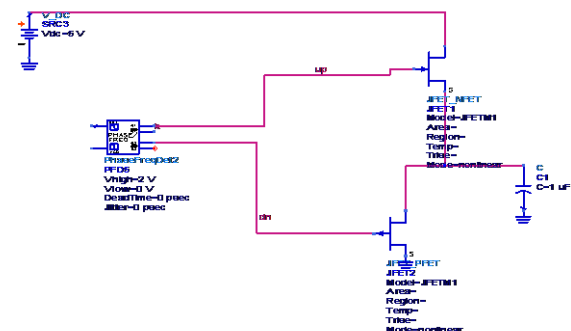


Fig. 4: implementation of the CP using JFET .

IV. MEMS Switches

MEMS refer to a 21st century technology named micro-electromechanical systems . MEMS are processes technology used to create tiny integrated devices or systems that combine mechanical, electrical and electronic components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimeters. These device systems have the ability to sense, control , actuate and generate on the macro scale [10]. In the most general form, MEMS consists of mechanical microstructures, micro-sensors, micro-actuators and microelectronics, all integrated onto the same silicon chip. Nowadays, MEMS have a diversity of applications across multiple markets like automotive, electronics, medical, communications, and defense weapons[11]. MEMS switches are surface-micro machined devices which use a mechanical movement to achieve a short circuit or an open circuit in the RF systems. RF MEMS switches are the specific micromechanical switches which are designed to operate for m 0.1 to 100 GHz [12]. With the recent exciting advancements in the field of miniaturized MEMS switch have shown to offer a superior RF performance in comparison to their semiconductor counterparts. [13-14]

IV. The PROPOSED MEMS CP

In Fig.5 an MEMS switch is replaced instead of GaAsFET Switch, that has a number of benefits. The channel charge and resistance are not found on the input voltage V_{in} , implying that distortion can be minimized., it results in a fast and low power circuit.

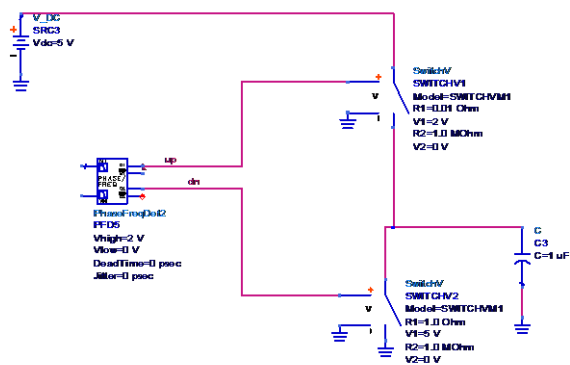


Fig. 5: implementation of the proposed MEMS CP.

The both circuits were simulated design at:

- Reference Freq. =50 MHz ,
wave form =sawtooth wave ,
voltage amplitude =1V,
feedback Freq. delay=2nsec, and
charging capacitor = 1 μ f

as illustrated in Fig.6

Reference signal leads divided VCO signal (feedback),
then output of the PFD voltage UP is high and DN is

low as shown in Fig.7. When UP is low and DN is high,
the voltage sink is active and voltage sinks into the load.

V. RESULTUS

Simulation results of the PFD are shown in Fig.5 which consists of up and down signals as outputs ,and reference and feedback signal as inputs. If the reference signal is leading feedback signal then up signal is high and varying from 0 to 2V , Fig.7 shows phase frequency detector output , down signal is constant in mV. These outputs are connected to CP to generate corresponding output.

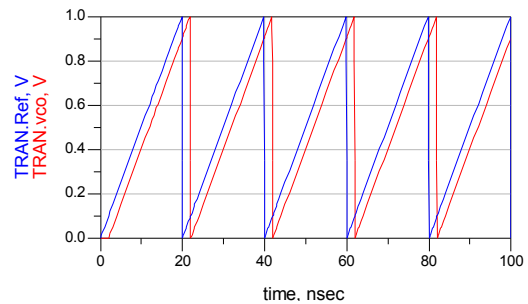


Fig. 6:Referance signal and delayed VCO signal

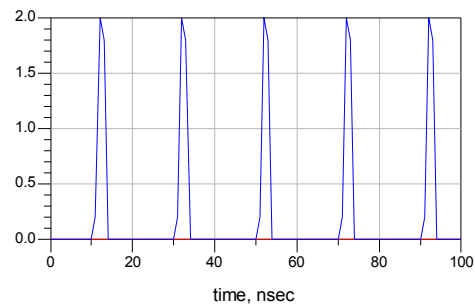


Fig. 7: Timing diagram of PFD up signals.

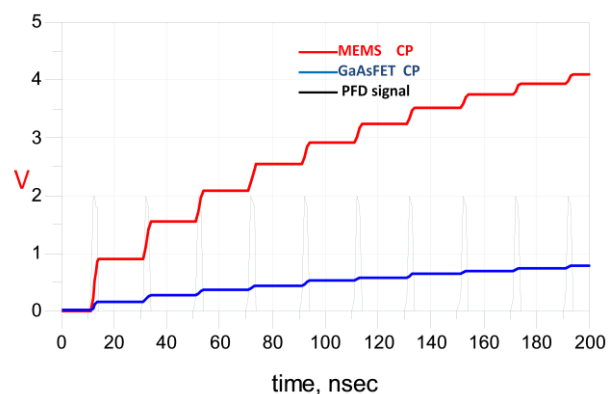


Fig. 8: Pumping-up of the proposed CP vs GaAFET CP

Fig. 8 shows combined output of phase frequency detector and charge pump when one of signal of PFD is high of proposed CP vs GaAFET CP

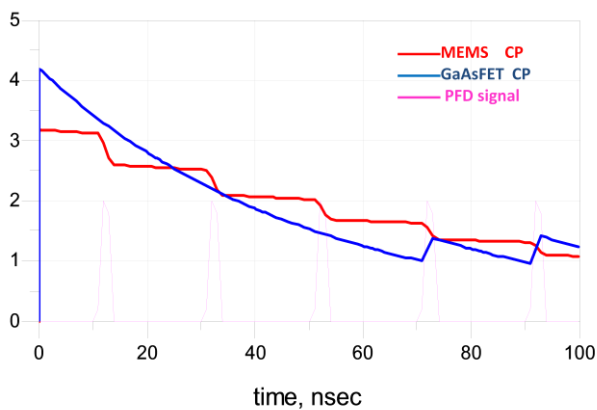


Fig. 9: Pumping-down of the proposed CP vs GaAFET CP

Table (1)insertion loss for GaAsFET switch vs MEMS switch

Time(nsec)	50	100	200
Devices			
GaAsFET (V)	0.274	0.525	0.783
MEMS (V)	1.55	2.92	4.1
ΔV	1.276	2.87	3.32
improvement %	25.5%	57.4%	66.3%

where

$$\text{improvement \%} = \frac{FET-MEMS}{input} * 100 \quad (2)$$

It can be notice that , The MEMS-CP proposed circuit can generate higher output voltage with 66.3% accuracy when compared with the MOS-CP devices

VII. CONCLUSION

The implementation introduced in this paper can perform much high performance charge pump circuit. The MEMS-CP proposed circuit can generate higher output voltage with 66.3% accuracy when compared with the MOS-CP devices. Power consumption is minimized. Additionally, this circuit does not has a problem with respect to Charge Injection.

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BIOGRAPHIES



Mazhar B. Tayel was born in Alexandria, Egypt on Nov. 20th, 1939. He was graduated from Alexandria University Faculty of Engineering Electrical and Electronics department class 1963. He published many papers and books in electronics, biomedical, and measurements. Prof. Dr. Mazhar Basyouni Tayel had his B.Sc. with honor degree in 1963, and then he had his Ph.D. Electro-physics degree in 1970. He had this Prof. degree of elect. and communication and Biomedical Engineering and systems in 1980. Now he is Emeritus Professor since 1999. From 1987 to 1991 he worked as a chairman, communication engineering section, EED BAU-Lebanon and from 1991 to 1995 he worked as Chairman, Communication Engineering Section, EED Alexandria. University, Alexandria Egypt, and from 1995 to 1996 he worked as a chairman, EED, Faculty of Engineering, BAU-Lebanon, and from 1996 to 1997 he worked as the dean, Faculty of Engineering, BAU - Lebanon, and from 1999 to 2009 he worked as a senior prof., Faculty of Engineering, Alexandria. University, Alexandria Egypt, finally from 2009 to now he worked

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