

Inter-chip Wireless Interconnect System over PCB Medium Channels

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Abstract— A design scheme is proposed for wireless interconnection communication between chips. The PCB medium channel is built with absorber layers. Two chip pin antennas are designed and simulated. Their scattering parameters are extracted and compared with three different cases. It evaluates the bit error rate (BER) performance via a interconnect communication model with a coherent binary phase shift keying (BPSK) modulator and demodulator. Simulation results show that the designed system performance degrades with the increase of separation distance and signal noise ratio. A high data rate at 1 Gb/s with a low BER $< 10^{-5}$ can be achieved with the transmitted power of 10 dBm.

Keywords— Inter-chip, Chip Pin Antenna, Binary Phase Shift Keying, Absorber Layer, Bit Error Rate

I. INTRODUCTION

With the increasing functions of very large scale integration (VLSI) circuit and advance in semiconductor technology, the pins in printed circuit board (PCB) are more and more intensive and the working frequency is also increasing, where the circuits are developed toward intensive, multi-layer and high-speed trend. When the working frequency of the bus connected to chips is greater than 10 GHz, the signal integrity issues become increasingly prominent, such as the reflection, crosstalk, delay, and the parasitic components [1, 2]. To solve these problems, (i) actively improve the traditional interconnect techniques, using low-resistivity conductor or low dielectric constant material, as well as three dimensional stacked structure; (ii) completely eliminate the dependence on wire interconnect and proposed different interconnect solutions, such as electromagnetic coupling, optical interconnect, and radio frequency technology [3-8].

In this paper, an inter-chip wireless interconnect communication system over PCB medium channel is designed. The PCB medium is coated with absorber layers. Based on these considerations, the open circuits of PCB medium can result in serious electromagnetic (EM) wave leakage, which leads to environmental EM pollution, especially for the case with a high-density, high-power circuit. It is believed that the leaky EM wave field intensity in this case without a shielding

wall can be much stronger than that generated from a cell phone, which could yield a serious healthy issue. In addition, the case for adding the metal walls becomes a cavity or a sort of parallel plate waveguide, which is currently not interested although it may prevent most signals.

The main idea of this paper is to demonstrate the validity of the concept of the system with a metamaterial absorber rather than complexing the system. It is found that when the number of more ports increases, the simulation time will dramatically increase. So two chip pins are applied as two ports during the scattering parameter simulation. It is sincerely believed that adding ports will only increase complexity and simulation time and will not deteriorate the concept due to the linearity of the propagation channels.

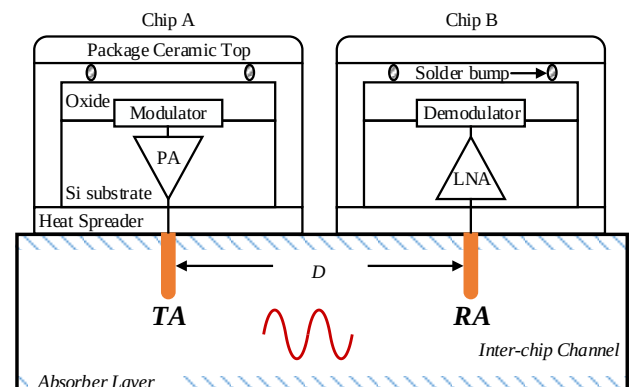


Figure 1. Inter-chip wireless interconnect design

The proposed solution for inter-chip wireless interconnect communication is shown in Figure 1. It consists of signal transmitter, signal receiver, and transmission channel. Herein, it mainly analyses the transmission channel between chip pin antennas, and constructs the simulation model. Compared the conventional applications, the inter-chip wireless interconnect communication system over PCB medium channel develops another function of chips' pins, and utilizes reasonably the free substrate. Meantime, the absorber materials are employed or explored to apply on the top and bottom surfaces of the

PCB substrate. Herein a sort of metamaterial is used to substitute the conceptual absorber material.

II. CHANNEL MODEL

The signal transmission from transmitting antenna (TA) to receiving antenna (RA) runs in the PCB medium, where the top and bottom surfaces are coated with an absorber layer. It ensures that the inter-chip power transfer is controlled in the PCB medium, and not disturbed by outside environment.

A. Absorber Layer

The absorber layer is currently a sort of metamaterial, which consists of a periodic structure. It is divided into three parts: periodic cell, dielectric substrate, and copper ground. Figure 2 shows partly the top view of an absorber layer, which has nine cells. The dielectric substrate is a FR-4 material with a relative permittivity of 4.4, a relative permeability of 1, loss tangent of 0.02, and the height of 0.2 mm.

The absorber layer assessment system was built up in a high frequency structure simulator (HFSS) environment, where the surrounding boundaries of a unit cell are truncated with the built-in Master and Slave boundary conditions, and two Floquet port excitations are added at the top and bottom wave ports. This setting of the absorber layer' unit cell is equivalent to a periodic, infinitely large absorbing structure. An EM plane wave is normally incident on the surface of the absorber layer with a transverse electric (TE) or transverse magnetic (TM) wave as shown in Figure 3.

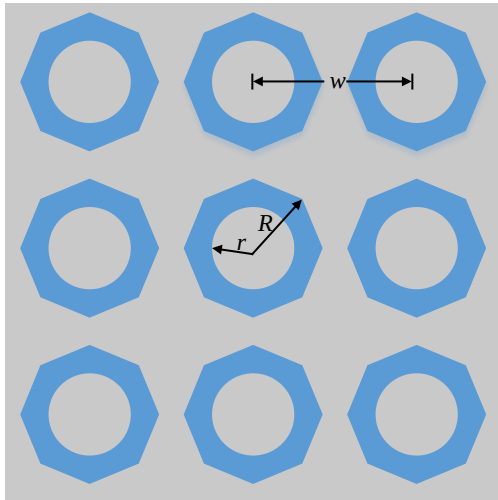


Figure 2. Top view of absorber layer, $w = 4.4$, $r = 1.5$, and $R = 1.8$, all in mm

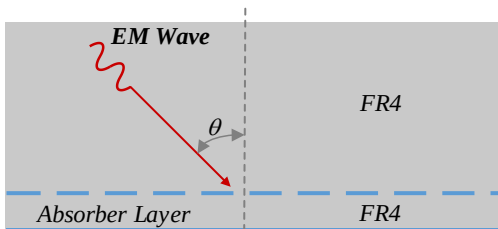


Figure 3. Side view of absorber layer and an incident EM wave

Actually, the absorber layer is not designed in a free space, but it is designed by using the PCB medium material of FR-4 as displayed in Figure 3. The absorptance $A(f)$ is a measure of the absorber layer's EM wave power absorption, which is precisely given as follows

$$A(f) = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (1)$$

where S_{11} and S_{21} are the reflection and transmission coefficients, respectively. Because the absorber is essentially shielded by the copper ground, the EM wave cannot penetrate the structure, i.e., $S_{21} = 0$.

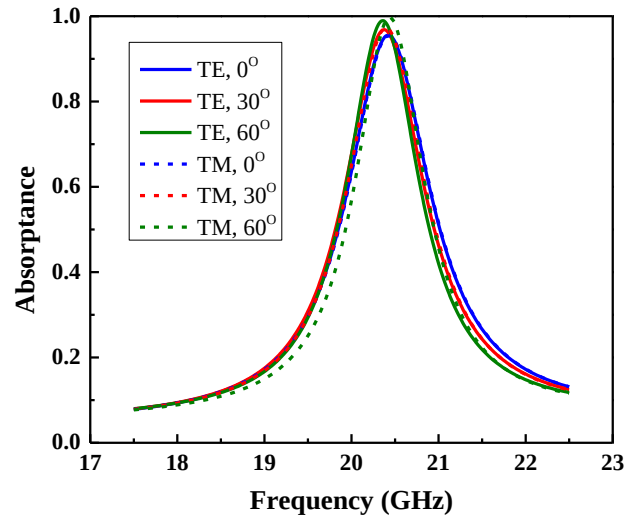


Figure 4. Magnitude of $A(f)$ with various incident angles for TE and TM polarizations

It is found that for the designed absorber layer the absorptance reaches 90% or greater in the frequency range of 20.27 through 20.58 GHz as seen in Figure 4. For both TE and TM polarizations, as θ continues to increase to 60°, $A(f)$ are essentially unchanged.

B. Scattering Parameters

The pins of every chip not only fix chip, but also can be used to radiate power. Herein they are designed as "chip pin antennas". Chip pin antenna (CPA) is approximately described as monopole antenna. Thus the length for TA and RA is determined by

$$l = \frac{1}{4} \cdot \frac{c}{f_0 \sqrt{\epsilon_r}} \quad (2)$$

where c is light speed in free space, ϵ_r is dielectric constant in PCB medium, and f_0 is carrier frequency of this designed communication system. Figure 5 shows the scattering parameters between TA and RA under three different circumstances over the PCB medium.

Case I refers to the PCB medium which is coated the absorber layers. As shown in Figure 5, the return loss of the CPA is -16.5830 dB at 20.4 GHz, and the bandwidth of -10

dB level range is from 19.7 to 21.2 GHz. Also, transmission coefficient between CPAs is -23.3866 dB at 20.4 GHz. In addition, Case II refers to the PCB medium which is covered with metal walls on top and bottom surfaces, Cases III refers that the top and bottom surfaces are open.

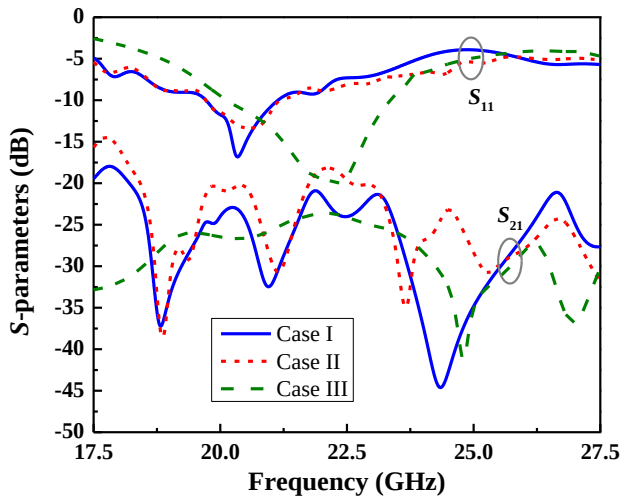


Figure 5. The S-parameters for the three different PCB medium channels

Compared with Case II, Case I can reduce CPA's return loss and improve their transmission coefficient. This is because the absorber layers absorb redundant waves, and reduce reflected waves and improve the EM environment in the PCB medium channel.

For Case I, S_{21} is determined by superposition of the direct propagation signals and the ground wall-reflected waves. The absorber layer is only able to absorb the reflected waves, and their frequencies are close to the centre frequency of the absorber layer. The S_{21} decreases outside the band is explained by the features of the grounded antenna system rather than the absorber performance in the frequency range. It is expected that the absorber bandwidth is further improved with a more complex structure or other special materials.

III. BER PERFORMANCE ANALYSIS

The scattering parameters are extracted from HFSS simulation model as a S2P file, which is imported into SNP component in Agilent ADS shown in Figure 6. The power amplifier (PA) and low noise amplifier (LNA) are respectively added in the input and output ports. The three parts are packed into wiicChannel module. Figure 7 shows the simulation schematic, which consists of data source, BPSK modulation, inter-chip channel, and BPSK demodulation. Then the BER performance is analysed.

Figure 8 shows the BER performance of the inter-chip wireless interconnect system for the case of the transmitted power at 10 dBm and the data rate of 1 Gb/s. Apparently, the BER performance degrades with the increase of the separation distance, D . It degrades from 1.82×10^{-5} at 28.3 mm to 9.45×10^{-4} at 45.3 mm.

As shown in Figure 9, the BER of the inter-chip wireless interconnect system is evaluated for the case of the transmitted power at 10 dBm and separate distance of 15 mm. In order to examine the system tolerance to noises, an additive white Gaussian noise (AWGN) source is added in wireless channel as shown in Fig. 7, which is a basic noise model used in information theory [9]. The simulated results indicate that the BER value decreases from 2.33×10^{-4} to 1.0×10^{-6} for $D = 15$ mm, when the signal to noise ratio (SNR) increases from 15 to 25. It is also found that when the noise is less than -128 dB, the BER maintains at a low level of 10^{-5} .

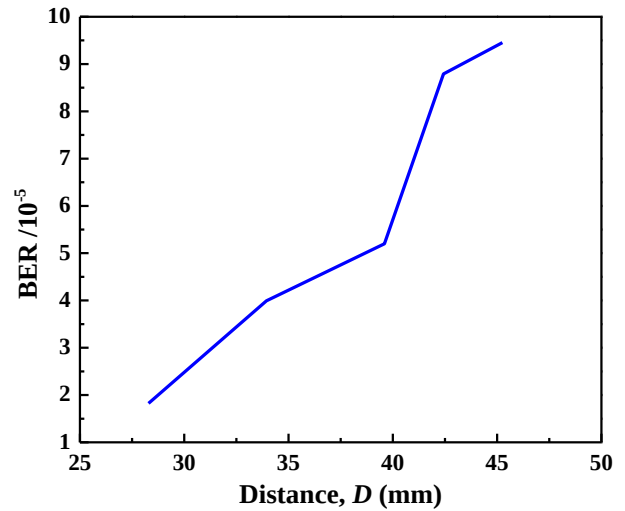


Figure 8. BER versus the TA-RA separation distance, D , with the data rate of 1 Gb/s

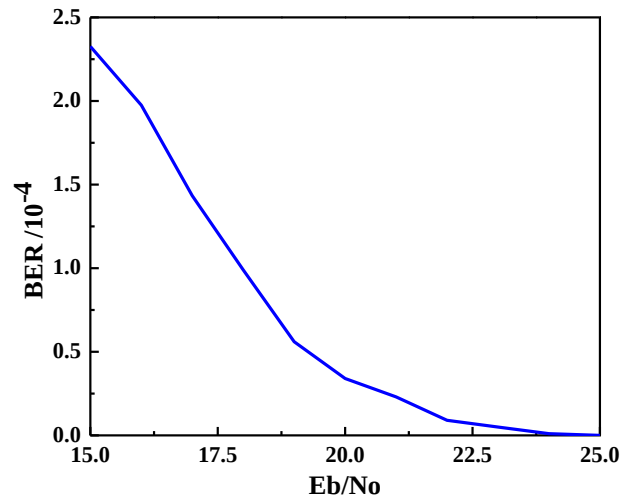


Figure 9. BER versus SNR with $D = 15$ mm

In addition, to achieve a high data rate with a low BER, one method is to increase the transmitted power, but it will result in a large power consumption and generate extra heat. Another method is to improve the transmission gain by inserting aluminium nitride layer and providing an efficient

means for heat removal. The third method is to use a channel-coding technique and share common RF front-ends.

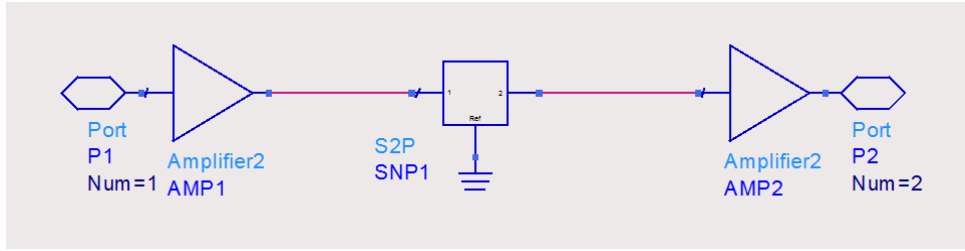


Figure 6. The wiicChannel module

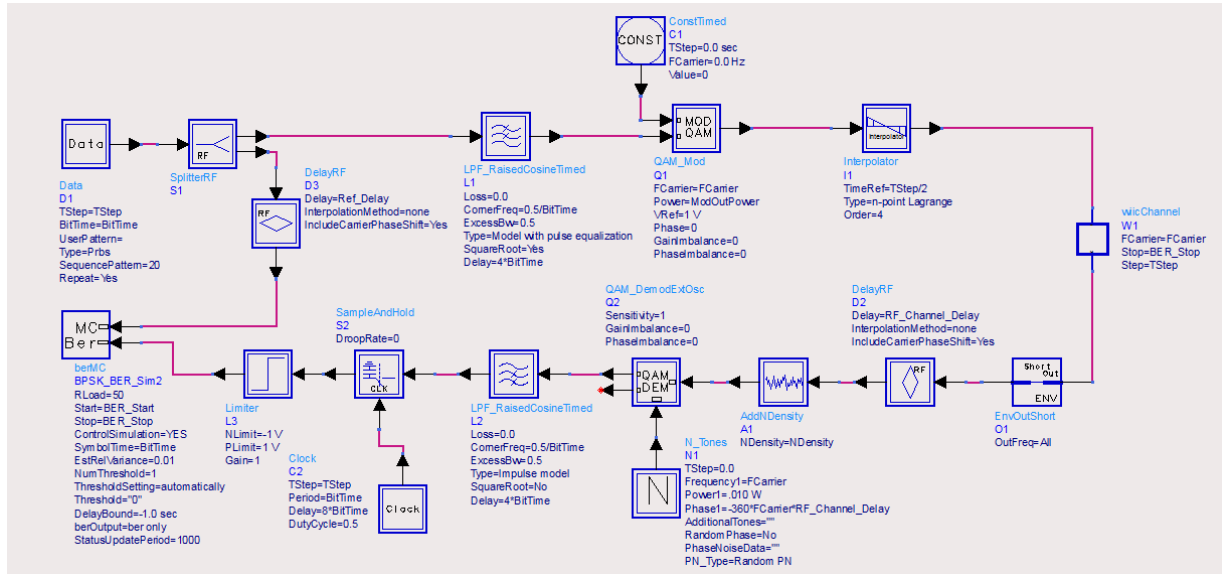


Figure 7. The ADS simulation schematic

IV. CONCLUSIONS

The novel interconnect scheme from one chip to another one is shown. The PCB medium channel with two absorber layers is studied, and has a better S-parameter performance by comparing with the case with two metal walls. The performance of coherent BPSK interconnect communication working at 20.4 GHz has been evaluated. It indicates that it is feasible for the inter-chip wireless interconnect design. A high data rate at 1 Gb/s with a low BER $< 10^{-5}$ is achievable with the transmitted power of 10 dBm. This research may provide a significant reference for VLSI design.

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