

Design of Two-stage Fully-integrated CMOS Power Amplifier for K-band Applications

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Abstract— This paper presents a K-band power amplifier integrated circuit using Samsung 65 nm CMOS process. The power amplifier adopts two-stage configuration for high power gain. The input, output, and inter-stage transformers are integrated. By neutralizing gate-drain capacitance using cross-coupled capacitors, the power gain and stability were improved. Its chip size is $0.78 \times 0.62 \text{ mm}^2$. The implemented two-stage power amplifier showed a power gain of 19.6 dB, a saturated output power of 13.5 dBm, and an efficiency of 7.19 % with a supply voltage of 1.1 V at the frequency band of 24 GHz.

Keywords— Differential power amplifier, integrated circuit, CMOS power amplifier, K-band, Cross-coupled capacitor (CCC)

I. INTRODUCTION

Recently, demands for short-range high-speed wireless communication systems have been increased. As a result, design of radio-frequency (RF) integrated circuits in mm-wave band becomes very important topic. For those wireless communications systems, design of a fully integrated power amplifiers (PAs) with reasonable performances is one of the major challenges.

Most of the PAs have been designed using compound semiconductor processes because of high efficiency and good linearity characteristics. However the compound semiconductor processes generally have poor integration

capability and high cost. As an alternative for the compound semiconductor processes, CMOS could be considered for the PA design. As the CMOS process have been advanced, the channel length of device gets shorter and shorter. Hence, their applications for high frequency circuits become possible. In addition, CMOS process has high integration capability and low cost. Therefore, CMOS PA design for next generation mobile communication systems, such as 5G, even in the mm-wave band becomes highly interesting topic for many circuit designers [1]-[8].

For wireless communication systems, the PAs must have high output power, wide bandwidth, high linearity, and high power gain. However, PA design using CMOS process is still challenging, since the transistors from sub-micron CMOS processes generally have low break down voltage, large parasitic components, and significant substrate loss.

In this paper, a fully-integrated two-stage differential PA is designed and implemented for K-band applications using Samsung 65 nm CMOS process. The designed PA have two-stage structure which consists of a drive stage and a power stage for high power gain. The gate-to-drain capacitances are compensated using cross-coupled capacitor (CCC) to improve power gain and stability of the PA. The transformers were designed based on the EM simulation to include the effect of the parasitic components.

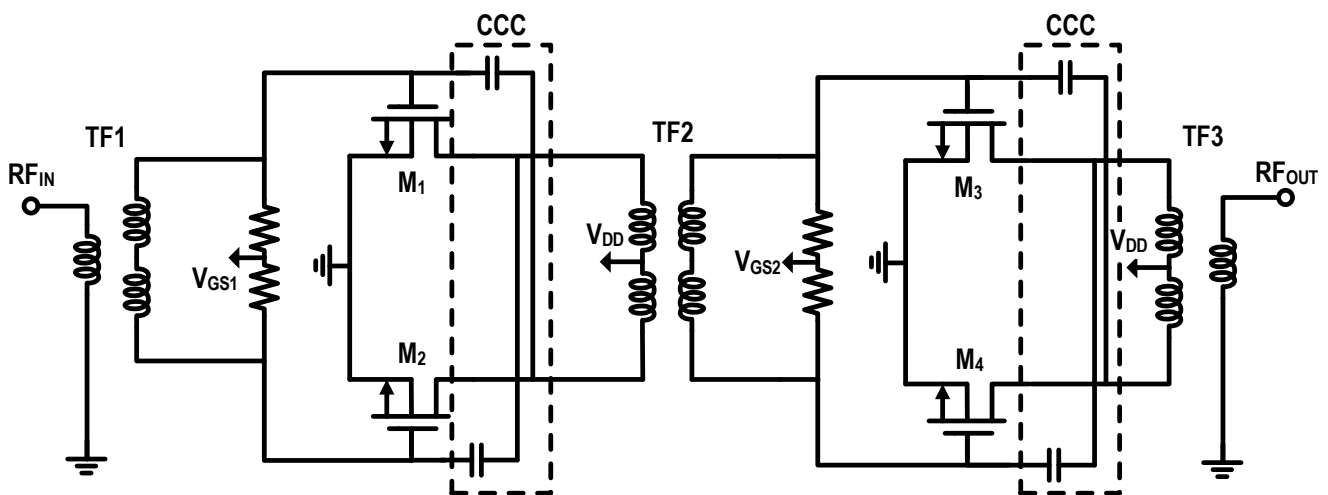


Figure 1. A schematic diagram of the two-stage differential CMOS power amplifier.

II. CIRCUIT DESCRIPTION

Figure 1 shows a schematic of the two-stage differential CMOS PA. The PA consists of a drive and power stages, cross-coupled capacitor (CCC) for gain and stability, and matching networks using transformers at the input, inter-stage, and output. Two-stage configuration was used for sufficient power gain of the PA. A differential structure for higher output impedance and more output power compared to the single-ended structure was adopted. The driver and power stages were designed with differential common-source (CS) structure with a supply voltage of 1.1 V.

Device sizes are important parameter for the performance of the PA. The device size is controlled by the gate width of the unit cell and multiplication number of the unit cell. The device size must be optimized in the trade-off between the output power and the power gain [9]-[11].

In this CMOS PA design, device sizes of the drive-stage and power-stage were optimized using source- and load-pull simulation. The device size for M1 and M2 of the drive-stage is a gate width of 260 μm and a gate length of 60 nm. In addition, the device size for M3 and M4 of the power-stage is a width of 400 μm and a length of 60 nm. A cross-coupled capacitors (CCC) using metal-insulator-metal (MIM) capacitors were adopted. The capacitance between the gate and drain of the device affects on the performances of the PAs. The gate-drain capacitance (C_{GD}) makes power gain, revers isolation, and stability factor worse. As a result, the CCCs were used to neutralize the C_{GD} 's at the drive- and power-stage, which can improve the power gain and stability of PA.

The transformers, TF1, TF2, and TF3, were used for impedance matching at the input, output, and inter-stage of the drive- and power-stages. To get the high coupling coefficient of transformer, the top-metal which have larger thickness was used for its primary and secondary turns. A planar structure was adopted because of the low leakage inductance and simplicity. However, it has high parasitic capacitances. Therefore, all transformers were designed based on EM simulations using ADS (Advanced Design System) Momentum to compensate for the effect of the parasitic passive components.

III. EXPERIMENTAL RESULTS

The two-stage differential PA is fabricated in Samsung 65 nm CMOS process. The chip micrograph is shown in Figure 2. The PA occupies a small area of 0.78x0.62 mm² including all pads with an active core area of 0.52x0.35 mm². This chip was measured by on-wafer probing. The measurements were carried out with a power supply of 1.1 V, and a DC current of 19 mA for the driver-stage, and 50 mA for the power-stage. Figure 3 shows the measured small-signal S-parameters of the PA. The small signal gain (S_{21}) is 16.34 dB and input return loss (S_{11}) is -13.49 dB at a frequency of 24 GHz.

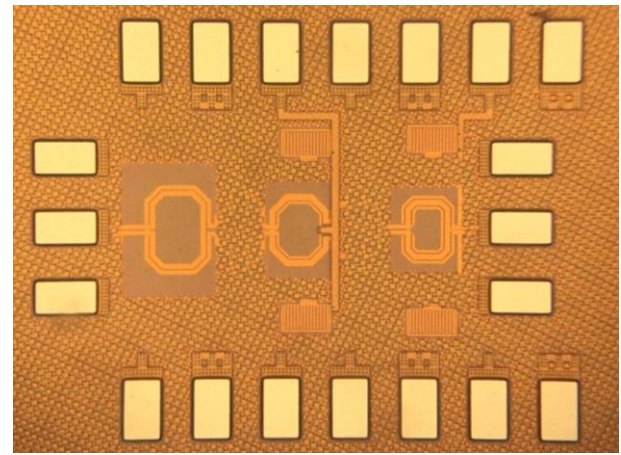


Figure 2. A microphotograph of the implemented K-band two-stage power amplifier.

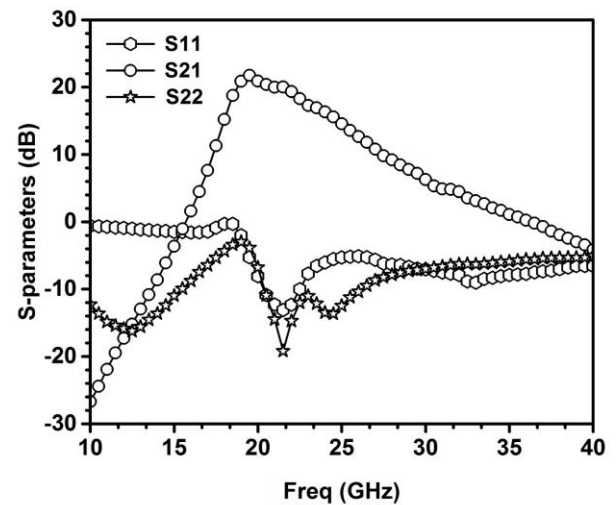


Figure 3. Measured S-parameters of the PA.

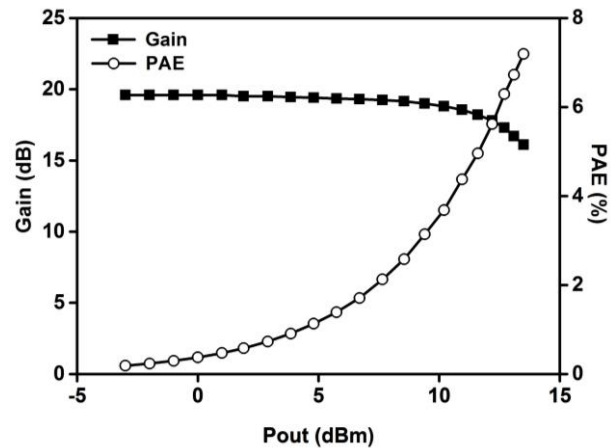


Figure 4. Measured power gain and PAE of the PA at the 24 GHz band.

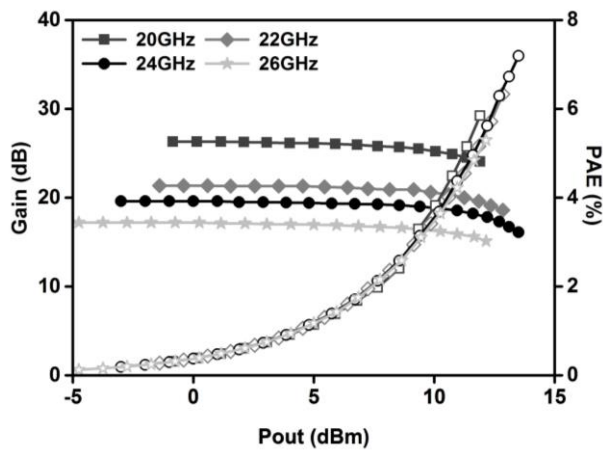


Figure 5. Measured power gain and PAE of the PA.

Figure 4 shows the measured power gain and power-added efficiency (PAE) according to the output power. The implemented PA exhibited a power gain of 19.6 dB, a saturated-output power (P_{SAT}) of 13.5 dBm, and an output 1dB compression point (P1dB) of 10.95 dBm. The PAEs of 4.37% and 7.19% at P1dB and P_{SAT} at the operational frequency band of 24 GHz, respectively.

The performances of the PA with a few selected frequencies were shown in Figure 5. The PA shows a power gain of more than 17.2 dB, P_{SAT} of more than 11.9 dBm, P1dB of 10.1 dBm, and efficiency of more than 12% in the frequency range of 20~26 GHz.

IV. CONCLUSIONS

In this paper, a two-stage differential CMOS power amplifier for the K-band application was designed and implemented. The chip was fabricated using Samsung 65 nm CMOS process. The input, output, and inter-stage transformers were integrated. In addition, the power gain and stability were improved using CCC. The implemented CMOS power amplifier delivered a high P1dB of 10.95 dBm, a power gain of 19.6 dB, and P_{SAT} of 13.5 dBm in which a PAE of 7.19% was achieved at the frequency of 24 GHz.

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