# Random-Permutation-Matrix-Based Cyclically-Coupled LDPC Codes

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***Abstract*—Cyclically-coupled quasi-cyclic low-density parity-check (CC-QC-LDPC) codes are a new class of QC-LDPC codes which can achieve excellent error performance and relatively low hardware requirement. In this paper, we modify the CC-QC-LDPC code construction by using random permutation matrices instead of circulant permutation matrices, forming the "random-permutation-matrix-based CC-LDPC (RP-CC-LDPC) code". The objective is to achieve a better error performance under the same code length. We simulate the bit error rate using FPGA simulations. We also compare the BER results and decoder complexity of the above codes with those of regular and irregular QC-LDPC codes under the same code length and code rate.**

***Index Terms*—Cyclically-coupled quasi-cyclic low-density parity-check, FPGA simulations, QC-LDPC, random-permutation-matrix-based CC-LDPC, RC-CC-QCLDPC.**

## I. Introduction

Low-density parity-check (LDPC) codes, introduced by Gallager [1], have been proved to have theoretical limits approaching the channel capacity. One set of methods to construct LDPC codes is based on random construction. Random constructions can produce LDPC codes that closely approach the Shannon capacity [2], [3], [4], [5]. In [2], [4], [5], the authors also gave some good irregular LDPC codes which had much better error performance than regular LDPC codes. Another set of ways is based on algebraic constructions. This kind of methods has attracted much interest because algebraic constructions yield structures that are strongly preferred in hardware implementations.

Quasi-cyclic LDPC (QC-LDPC) codes are a particular important class of algebraic-constructions-based LDPC codes. QC-LDPC codes have been widely used because of their flexible design and ease of implementation. We can use different structured codes to construct QC-LDPC codes, such as finite-geometry codes [6] and circulant-permutation-matrix (CPM) based codes [7],[8],[9]. It is also well-known that short cycles existing in the Tanner graphs of LDPC codes will degrade the error performance. They may also form structures such as stopping sets [10],[11], elementary/dominant/detrimental trapping sets [12], [13], [14] and absorbing sets [15], [16], [17] which raise the error floor in the high signal-to-noise (SNR) region.

In order to optimize the performance of QC-LDPC codes, short cycles should be removed during code constructions. However, structured codes usually cannot guarantee a large girth (shortest cycle length) with a relatively short code length. The progressive-edge-growth (PEG) algorithm is a popular method to construct LDPC codes [18],[14]. It also cannot guarantee achieving the largest possible girth when used in constructing QC-LDPC codes. Hence error floors can still exist in the high SNR region for codes constructed under such a method [19].

Some efficient computer searching methods have been proposed to remove the short cycles in QC-LDPC codes. Since there is an enormous number of possible cycle combinations, it is extremely time-consuming and infeasible to conduct an exhaustive computer search. The hill-climbing algorithm [20] is an effective searching method that modifies the elements in the base matrix iteratively. In [21], a fast hill-climbing method has been further proposed to reduce the time complexity and make the searching method more efficient.

Using LDPC convolutional codes (LDPCCCs) and QC-LDPC convolutional codes (QC-LDPCCCs) is another way to improve the error performance and lower the error floor [22],[23],[24]. However, the decoder of LDPCCC has a high hardware complexity. A novel type of LDPC block codes which called "cyclically-coupled quasi-cyclic LDPC codes" (CC-QC-LDPC codes) has been proposed recently [25]. This kind of codes is constructed by cyclically connecting a number of QC-LDPC sub-codes. It has a similar error performance and higher throughput compared with the LDPCCCs but allows a much simpler decoder design. In [25], the authors construct a girth-8 CC-QC-LDPC code with a rate of 5/6 and length 98304. The decoder of the CC-QC-LDPC code has been implemented on a field-programmable-gate-array (FPGA) device and achieve a throughput of 3.0 Gb/s. In [26], a novel type of QC-LDPC codes which can achieve the same girth with a shorter code-length has been proposed and studied.

In this paper, we modify the CC-QC-LDPC code and propose a new type of CC-LDPC codes. Instead of using circulant permutation matrices, we make use of random permutation matrices to form the basic building blocks of CC-LDPC codes. The proposed code is called "random-permutation-matrix-based CC-LDPC (RP-CC-LDPC) code". The decoder of the proposed RC-CC-LDPC codes has been implemented using FPGA. The error performance and decoder complexity of the new code are evaluated and compared with other codes.

We organize this paper as follows. In Section II, we review the structure of QC-LDPC and CC-QC-LDPC codes. We also describe the equations governing the cycles of the codes. In Section III, we describe the structure of the proposed RP-CC-LDPC codes. Finally, we show and compare the simulation results in Section IV.

## II. QC-LDPC Codes and CC-QC-LDPC Codes

A $(J, L)$ regular QC-LDPC code can be described by a parity-check matrix $\mathbf{H}$

$$\mathbf{H} = \begin{bmatrix} \mathbf{I}_{(p_{0,0})} & \mathbf{I}_{(p_{0,1})} & \cdots & \mathbf{I}_{(p_{0,L-1})} \\ \mathbf{I}_{(p_{1,0})} & \mathbf{I}_{(p_{1,1})} & \cdots & \mathbf{I}_{(p_{1,L-1})} \\ \cdots & \cdots & & \cdots \\ \mathbf{I}_{(p_{J-1,0})} & \mathbf{I}_{(p_{J-1,1})} & \cdots & \mathbf{I}_{(p_{J-1,L-1})} \end{bmatrix} \quad (1)$$

where $\mathbf{I}_{(p_{j,l})}$ represents a $z \times z$ circulant permutation matrix (CPM) obtained by cyclically right-shifting the $z \times z$ identity matrix $\mathbf{I}$ by $p_{j,l}$ positions ($0 \le j \le J-1, 0 \le l \le L-1, 0 \le p(i,j) \le z-1$). $\mathbf{I}_{(p_{j,l})}$ represents the $z \times z$ identical matrix $\mathbf{I}$ when $p_{j,l} = 0$. Therefore, QC-LDPC codes also can be defined by a $J \times L$ base matrix $\mathbf{H}_b$:

$$\mathbf{H}_b = \begin{bmatrix} p_{0,0} & p_{0,1} & \cdots & p_{0,L-1} \\ p_{1,0} & p_{1,1} & \cdots & p_{1,L-1} \\ \cdots & \cdots & & \cdots \\ p_{J-1,0} & p_{J-1,1} & \cdots & p_{J-1,L-1} \end{bmatrix} \quad (2)$$

For a QC-LDPC code, an arbitrary cycle of length $2i$ has to pass through $2i$ elements of the base matrix. The sequence of the elements are denoted by $(j_0, l_0), (j_0, l_1), (j_1, l_1), ..., (j_{i-1}, l_{i-1}), (j_{i-1}, l_0)$, where $j_s \neq j_{s+1}$ and $l_s \neq l_{s+1}$ for $0 \le s-1 \le i$. Then there exists a cycle of length $2i$ if [21]

$$\sum_{s=0}^{i-1} (p_{j_s,l_s} - p_{j_s,l_{s+1}}) = 0 \pmod z. \quad (3)$$

In [25], cyclically-coupled QC-LDPC (CC-QC-LDPC) codes based on cyclically coupling several identical QC-LDPC sub-codes have been proposed. Denoting a QC-LDPC sub-code $\mathbf{H}_s$ as

$$\mathbf{H}_s = \begin{bmatrix} \mathbf{H}_l & \mathbf{H}_m & \mathbf{H}_r \end{bmatrix}, \quad (4)$$

the parity-check matrix of a CC-QC-LDPC code can be written as

$$\mathbf{H}_{cc} = \begin{bmatrix} \mathbf{H}_l^1 & \mathbf{H}_m^1 & \mathbf{H}_r^1 & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{H}_l^2 & \mathbf{H}_m^2 & \mathbf{H}_r^2 & \cdots & \mathbf{0} & \mathbf{0} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \mathbf{H}_r^K & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{H}_l^K & \mathbf{H}_m^K \end{bmatrix} \quad (5)$$

where $K$ sub-codes have been coupled in a cyclic manner. In (5) and in the remaining paper, $\mathbf{0}$ denotes an all-zero matrix of appropriate size. Both $\mathbf{H}_l$ and $\mathbf{H}_r$ are of the same size and are assumed to consist of $J \times W$ CPMs whereas $\mathbf{H}_m$ consists of $J \times (L - 2W)$ CPMs. $W$ which represents the number of coupled block columns is also called the "coupling degree". In [25], both $J$ and $W$ equal 4 and $L$ equal 28, which means both $\mathbf{H}_l$ and $\mathbf{H}_r$ have 4 block rows and 4 block columns, and $\mathbf{H}_m$ has 4 block rows and 20 block columns.

A CC-QC-LDPC decoder contains $K$ identical sub-decoders and a global controller. The $K$ sub-decoders are connected in a cyclic way and each of them corresponds to a sub-code $\mathbf{H}_s$. Moreover, check-to-variable (C2V) messages and variable-to-check (V2C) messages are to be passed between consecutive sub-decoders. By using such a decoder design, the throughput of decoder is approximately the sum of the throughput of the sub-decoders.

## III. Proposed Permutation-Matrix-Based CC-LDPC (RP-CC-LDPC) Codes

We again consider the same sub-code (4) in which both $\mathbf{H}_l$ and $\mathbf{H}_r$ contain $4 \times 4$ sub-matrices and $\mathbf{H}_m$ contains $4 \times 20$ sub-matrices. However, instead of CPMs, random permutation matrices are used in the sub-matrices. We can also view the modified $\mathbf{H}_s$ as a protograph-based LDPC code [27] with a base matrix $\mathbf{B}_s$ given by

$$\mathbf{B}_s = [\mathbf{1}_{4\times4} \;\; \mathbf{1}_{4\times20} \;\; \mathbf{1}_{4\times4}] \quad (6)$$

where $\mathbf{1}_{4\times4}$ and $\mathbf{1}_{4\times20}$ represent the $4 \times 4$ and $4 \times 20$ all-one matrices, respectively. The corresponding CC-LDPC codes constructed from $\mathbf{B}_s$, which we called "random-permutation-matrix-based CC-LDPC (RP-CC-LDPC)" codes, are therefore represented by the base matrix $\mathbf{B}_{cc}$

$$\mathbf{B}_{cc} = \begin{bmatrix} \mathbf{1}_{4\times4} & \mathbf{1}_{4\times20} & \mathbf{1}_{4\times4} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{1}_{4\times4} & \mathbf{1}_{4\times20} & \mathbf{1}_{4\times4} & \cdots & \mathbf{0} & \mathbf{0} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \mathbf{1}_{4\times4} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{1}_{4\times4} & \mathbf{1}_{4\times20} \end{bmatrix}. \quad (7)$$

By replacing each 1 in $\mathbf{B}_s$ by a random permutation matrix of size $z \times z$ and then substituting the results into $\mathbf{B}_{cc}$, RP-CC-LDPC codes are obtained.

## IV. Results

We consider a RP-CC-LDPC code with $J = 4$, $L = 28$, $W = 4$, $K = 4$ and $z = 1024$. As we mention earlier, permutation matrices are randomly generated for the RP-CC-LDPC code. We compare the bit error performance and hardware complexity of our proposed RP-CC-LDPC code with other LDPC codes. All codes have the same code rate $5/6$ and code length 98304, and are simulated under an additive white Gaussian noise (AWGN) channel. All our results are generated by FPGA implementation of the corresponding decoders at a clock frequency of 100 MHz and 4-bit quantization.

### A. Comparison with CC-QC-LDPC Code

First, we compare our RP-CC-LDPC code with the CC-QC-LDPC code reported in [25]. Fig. 1 shows that the proposed RP-CC-LDPC code outperforms the CC-QC-LDPC code in terms of bit error rate (BER). In particular, RP-CC-LDPC code outperforms CC-QC-LDPC code by 0.05 dB at a BER of $10^{-13}$. No error floor is also observed above this BER level.

Table IV compares the complexity and throughput of the two decoders. The CC-QC-LDPC code and RP-CC-LDPC code are represented by Code C and Code D, respectively. As

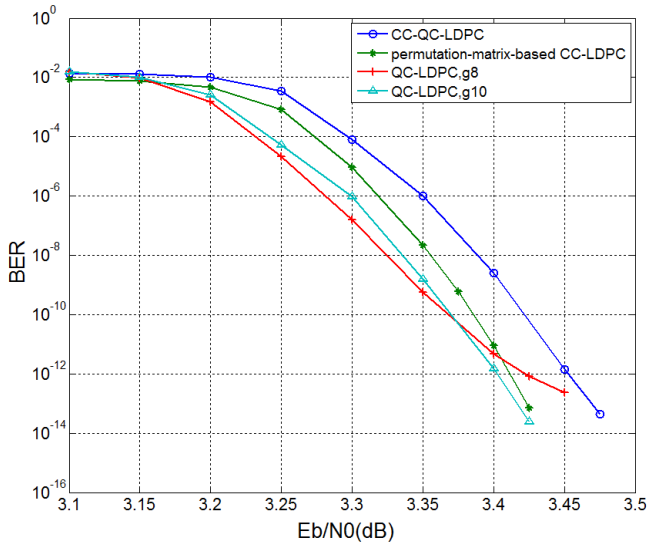


Fig. 1. The bit error rate (BER) comparison of different codes. All the results are obtained from FPGA simulations under an AWGN channel and 4-bit quantization.

TABLE I
HARDWARE INFORMATION OF THE DECODER IMPLEMENTATIONS.
CODE A: $4 \times 24$ REGULAR QC-LDPC CODE, GIRTH=8, $z = 4096$;
CODE B: $4 \times 24$ IRREGULAR QC-LDPC CODE, GIRTH=10, $z = 4096$;
CODE C:$16 \times 96$ CC-QC-LDPC CODE, GIRTH=8, $z = 1024$;
CODE D: $16 \times 96$ RP-CC-LDPC CODE, $z = 1024$.

| Code | A | B | C | D |
|---|---|---|---|---|
| Parallelism degree | 32 | 32 | 32 | 4 |
| ALUTs | 65,178 | 55,990 | 70,342 | 31,660 |
| Registers | 53,36 | 41,740 | 43,801 | 13,564 |
| Memory bits | 1,769,372 | 1,474,560 | 2,359,296 | 4,297,289 |
| Clock | 100 MHz | 100 MHz | 100 MHz | 100 MHz |
| Throughput | 1.55 Gbps | 1.55 Gbps | 1.55 Gbps | 0.182 Gbps |

we can observe, the degree of parallelism of the RP-CC-LDPC code is reduced by 8 times compared with that of the CC-QC-LDPC code. The main reason is the random permutation matrices being used in the RP-CC-LDPC code. Consequently, the same ratio in terms of decoder throughput is observed. We can also see a substantial increase of memory required in the RP-CC-LDPC decoder. They are used to store the entries of the permutation matrices which are random in general.

### *B. Comparison with Regular and Irregular QC-LDPC Codes*

We construct a $4 \times 24$ QC-LDPC code with $z = 4096$. Using the fast hill-climbing algorithm in [21] and illustrated in 2, we can eliminate both cycle-4 and cycle-6 but not cycle-8. The largest girth that we can obtain is therefore 8. The resultant $4 \times 24$ QC-LDPC code is denoted as Code A in Table IV. In order to achieve a larger girth, we assign 4 all-zero sub-matrices for each row in a $4 \times 24$ QC-LDPC code. Thus, all block rows have a weight of 20, 16 block columns have a weight of 3 and 8 block column have a weight of 4. The structure of the resultant irregular QC-LDPC code is shown in 3 and is denoted as Code B in Table IV. Each $\phi$ in 3 represents an all-zero sub-matrix. Again we apply the fast

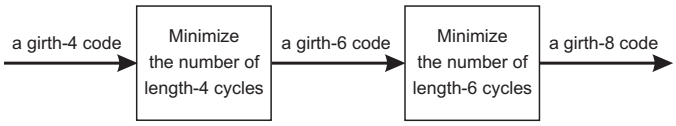


Fig. 2. Fast hill-climbing algorithm [21].

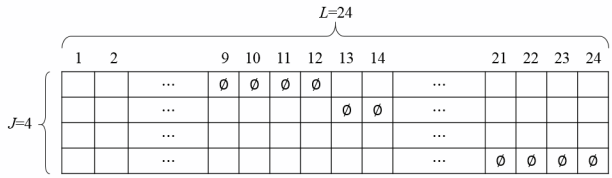


Fig. 3. Structure of the irregular QC-LDPC code.

hill-climbing algorithm and we are able to eliminate all cycle-4, cycle-6 and cycle-8. A girth-10 irregular QC-LDPC code is hence obtained.

Referring to Fig. 1, the BER curves show that both the regular and irregular can outperform the proposed RP-CC-LDPC code in the low $E_b/N_0$ region. However, an error floor occurs at around $10^{-13}$ BER for the regular QC-LDPC code. It is probably due to the cycle-8 in the code. At $E_b/N_0 = 3.425$ dB, the BER performances of irregular QC-LDPC code and RP-CC-LDPC code are very similar. The BER curve trends seem to forecast that the irregular QC-LDPC code will be outperformed by RP-CC-LDPC code beyond $E_b/N_0 = 3.45$ dB. That needs to be verified though. Table IV compares the complexity and throughput of the decoders. Again, the RP-CC-LDPC code is at a disadvantageous position in terms of decoder complexity and throughput.

## V. CONCLUSION

We have proposed a random-permutation-matrix-based cyclically-coupled LDPC (RP-CC-LDPC) code. We have compare its performance with the CC-QC-LDPC code, regular and irregular QC-LDPC codes using FPGA simulations. Results show that the BER performance of the RP-CC-LDPC code is comparable to and can possibly exceed that of other codes. However, decoder complexity and throughput are major issues of the RP-CC-LDPC code which makes use of relatively more complex random permutation matrices instead of simple circulant permutation matrices. Our future work will include designing CC-LDPC codes with a lower complexity than RP-CC-LDPC codes but at the same time achieving good BER performance.

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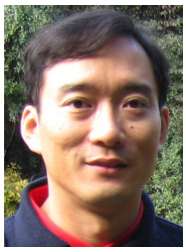

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