

Design of CMOS Continuous-Time Low-pass Delta-Sigma Modulator for Digital Distributed Antenna System based on IF-over-Fiber Transmission

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Abstract—A CMOS continuous-time low-pass delta-sigma modulator (DSM) circuit that digitizes an analog mobile signal at 10 MHz intermediate frequency (IF) in a digital distributed antenna system (DAS) with IF-over-fiber scheme is designed in this paper. Detailed design processes and results from system to circuit levels are provided, which is helpful for the design of a DSM circuit for another digital DAS system based on DSM technique. The simulated peak signal-to-noise and distortion ratio of the designed DSM circuit was 49.4 dB, and high stop-band rejection ratios were achieved by exploiting the zero optimization technique in the noise transfer function of the designed DSM.

Keywords— DAS, DSM, IFoF, RoF

I. INTRODUCTION

According to recent research, almost 80% of mobile data traffic is generated in building [1]. Therefore, the importance of delivering mobile service to in-building users is being magnified. Among several candidates for the in-building mobile communication service, distributed antenna system (DAS) shown in Figure 1 has attracted widespread interests recently [1-4]. This is because it offers better coverage without interference between cells.

However, because the conventional DAS system is based on analog radio-over-fiber (RoF) architecture, the mobile signal at radio frequency (RF) is translated into a lightwave signal at the DAS transmitter and transported to the DAS receiver where the received optical signal is transformed back to the electrical signal, amplified and finally transmitted in the air through antenna. Therefore, the electrical-to-optical (E/O) converter at the DAS transmitter and the optical-to-electrical (O/E) converter at the DAS receiver must have high linearity over a frequency range up to the RF carrier frequency [5]. Not only that, but the analog RoF system also suffers from the signal-to-noise ratio (SNR) reduction in proportion to high split ratios for DAS receivers and the optical transmission distance. Accordingly, there have been approaches that digitize the mobile RF signal and, thus, use digital E/O and O/E converters, which in turn considerably mitigate the analog RoF issues.

Recently, a digital intermediate frequency-over-fiber (IFoF) system using low-pass delta-sigma modulation to quantize the analog mobile signal has been proposed and showed the

effectiveness of the system [6], as shown in Figure 2. However, the previous work is mainly focused on the optical transmission system not the delta-sigma modulator (DSM) used in the link.

In this paper, more detailed design results of the continuous-time low-pass DSM used in the digital IFoF (D-IFoF) transmission system are provided. Both system and circuit-level design processes are provided through this paper.

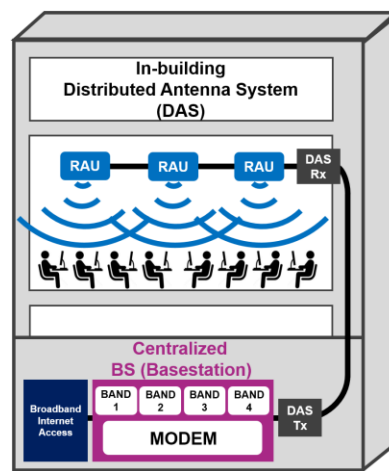


Figure 1. In-building DAS system architecture

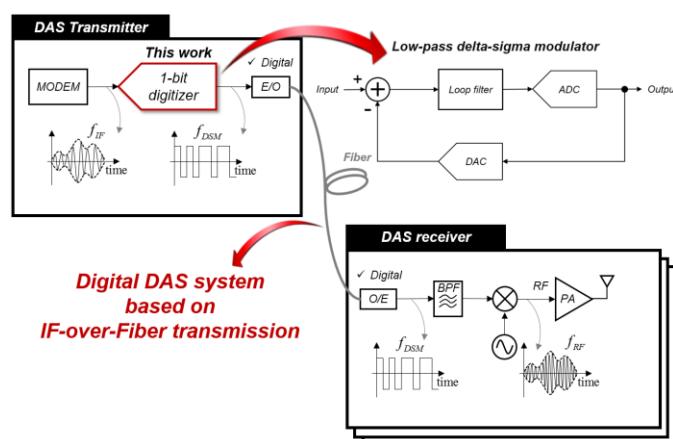


Figure 2. DSM-based digital IFoF transmission system

II. SYSTEM-LEVEL DESIGN OF DSM

A. Continuous time vs Discrete time implementation

There are two options for implementing a DSM circuit: continuous time (CT) and discrete time (DT) modulators. Each of them has its own advantages and disadvantages. However, in terms of bandwidth and power consumption, the continuous-time implementation is a more appropriate choice. Advantages of CT and DT DSMs are described in Table 1.

TABLE 1. ADVANTAGES OF CT AND DT DSM IMPLEMENTATIONS

Advantages of CT DSM	Advantages of DT DSM
✓ Inherent anti-aliasing filter	✓ Robust against clock jitter
✓ Relaxed OP amp bandwidth requirement	✓ Robust against excess loop delay
✓ Higher sampling frequency possible	✓ Robust against DAC waveform shape
✓ Robust against glitch	✓ Accurate integrator transfer function

Owing to the lower speed requirement, CT scheme has been chosen for the DSM in this paper because the sampling rate of the DSM is 622.08 MHz for optical carrier (OC) 12 and the gain-bandwidth product of the OP amp in the DSM has to be higher than 1 to 1.5 times the sampling frequency in CT implementation.

B. System-level design

The noise transfer function (NTF) determining the behaviour of the DSM in frequency domain was designed. Because the carrier frequency of the analog long-term evolution (LTE) signal for transmit over the D-IFoF link was 10 MHz and the LTE signal bandwidth was 9 MHz with 50 resource blocks, the LTE signal occupied from 5.5 MHz to 14.5 MHz and, thus, the low and high stop bands were direct current (DC) – 5.5 MHz and 14.5 MHz – 20 MHz, respectively. For a reasonable adjacent channel leakage ratio (ACLR) of the LTE signal, the bandwidth of 20 MHz was selected for loop filters in the DSM.

Figure 3 depicts the signal-to-quantization noise ratio with several design parameter sweeps. From the simulation result, the order of the DSM and oversampling ratio (OSR) was selected as 3rd-order and 15.55, respectively. Figure 4 shows the designed NTF with the parameters mentioned above with the MATLAB DSM toolbox. As shown in the figure, because the amount of quantization noise slightly above the IF frequency range (dotted area) was quite large, the quality of the delta-sigma digitized LTE IF signal components especially at high frequencies was considerably deteriorated, and the requirements of a band-pass filter for the signal reconstruction must be very stringent to suppress the large amount of noise.

To relieve the high quantization noise issue, the zero optimization technique making the zeros of the NTF transfer function to be optimally separated out from each other to obtain better signal quality performance, has been applied to the present DSM. However, the aim of the technique in our DSM is slightly different than that of the traditional scheme because the locations of NTF zeros in our modulator have

been optimized not only for the in-band signal quality but also for noise reduction at the guard bands. Accordingly, the modified NTF in the z-domain was designed as follows:

$$\frac{(z-1)(z^2-1.976z+1)}{(z-0.6654)(z^2-1.523z+0.6597)} \quad (1)$$

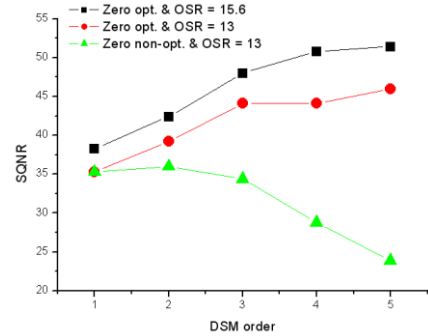


Figure 3. Simulated SQNR vs the number of DSM order and OSR values

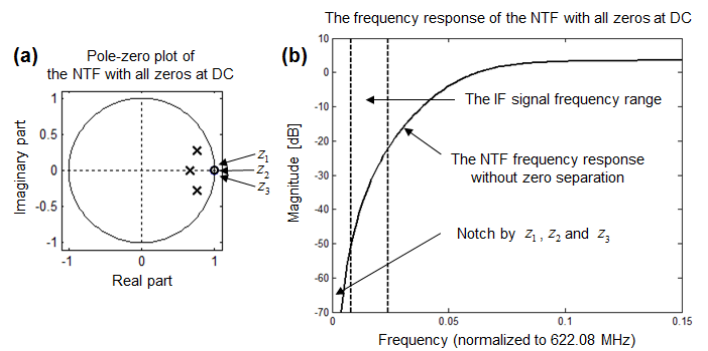


Figure 4. Designed NTF of the developed 622 MHz 3rd-order low-pass DSM with all zeros at DC: (a) pole-zero plot and (b) frequency response

The frequency response of the final NTF is represented by the solid line in Figure 5. In Eq. (1), zeros are located at z_1 , z_2 and z_3 of 1 and $0.988 \pm j0.1545$ with their phases of 0 and ± 0.1551 radian, respectively. Since the sampling frequency of the DSM is 622.08 MHz ($= 2\pi$ in radian in the z-domain), the corresponding frequencies of those NTF zeros of z_1 , z_2 and z_3 are DC and ± 15.36 MHz, respectively, indicating that the quantization noise notches of the designed DSM occur at those zero frequencies.

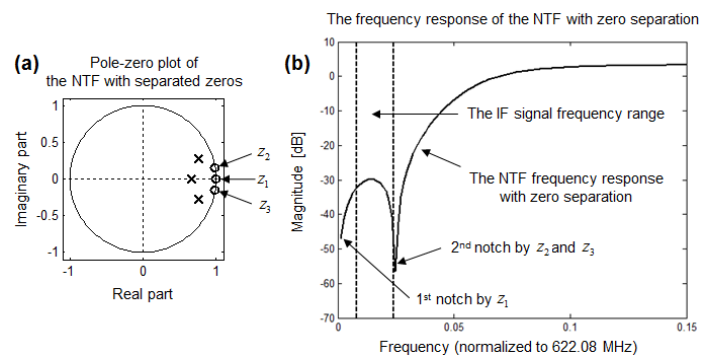


Figure 5. Designed NTF of the developed 622 MHz 3rd-order low-pass DSM with zero separation: (a) pole-zero plot and (b) frequency response

III. CIRCUIT-LEVEL DESIGN OF DSM

As mentioned before, the DSM output pulse train is applied to the lightwave transceivers for OC-12 data rate. This means that the proposed system does not require any additional blocks between the DSM and the optical transmitter or, more importantly, any rate-specific custom optical transceivers, whereas the transmission rate of the previous band-pass sampling-based DRoF optic link is mainly determined by the multiplication of the sampling frequency and the number of resolution bits of the ADC located in the CU of the DRoF link. It is apparent that it is not easy for the multiplication value to perfectly match the transmission rate of standard optical transceivers such as OC-12 up to 622.08 Mbps, OC-24 of 1244.16 Mbps and the speeds of OC-48 of up to 2488.32 Mbps, because the sampling frequency and the number of bits of the ADC and DAC in the DRoF system are strongly dependent on frequencies of RF signals and the required signal quality for the transmission, respectively.

Figure 6 shows the circuit block diagram of the designed DSM with parameter values. R1 in Figure 6 (a), is the most important block in the DSM because the resistor R1 mainly determined the amount of the thermal noise and the thermal-noise limited SNR. The resistor can be calculated according to the following equation:

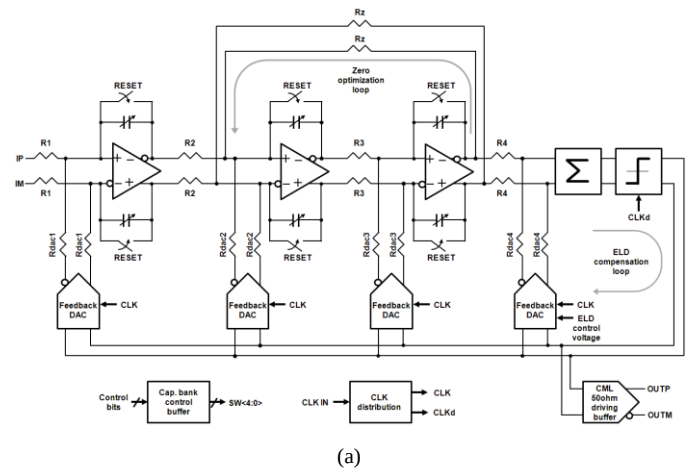
$$R1 \approx \frac{\frac{V_{in}^2}{2}}{32KTf_B \cdot 3 \cdot 2^{2B-1}} \quad (2)$$

where $V_{in}=0.25$ V (common-mode to one peak voltage, peak-to-peak 0.5 V), $f_B=20$ MHz, $B=9.3$ bit (for $SNR_{thermal}=56$ dB), $K=1.38e-23$, and $T=300$ K.

With the Eq. (2), R1 can be calculated as approximately 20 kohm with $SNR_{thermal}$ of 56 dB which is roughly 7 dB higher than the designed peak SQNR of 49 dB. Therefore, the DSM was designed to be more likely to be quantization noise-limited system. Other resistor and capacitor values were extracted from the designed NTF with the cascade of integrator and feedback structure termed CIFB. For excess loop delay compensation, a fast feedback loop around the quantizer was added and improved the overall feedback DSM loop stability. In Figure 6 (b), the initial values of the parameters for the DSM and their final values are summarized.

As depicted in Figure 7, the capacitors of C1, C2 and C3 were implemented as capacitor banks whose capacitance are controlled by 5 bit control word, SW<4:0>, with a minimum step of 25 fF. The capacitors used in the banks were metal-insulator-metal capacitors provided by the foundry.

To drive a 50 ohm load, a current mode logic (CML) buffer was designed to operate at the high frequency of 622.08 MHz. The output signal of the CML buffer drives the E/O converter and is then converted into a digital optic pulse train to be transmitted over the D-IFoF link.



Initial value		Final value	
Parameter	Value	Parameter	Value
R1	20 kohm	R1	17 kohm
R2	9.4 kohm	R2	7 kohm
R3	13.5 kohm	R3	9 kohm
C1	623 fF	C1	750 fF
C2	500 fF	C2	750 fF
C3	500 fF	C3	750 fF
Rdac1	20 kohm	Rdac1	17 kohm
Rdac2	14.7 kohm	Rdac2	11 kohm
Rdac3	20.8 kohm	Rdac3	13 kohm
Rz	31.3 kohm	Rz	23 kohm

Figure 6. Circuit block diagram of the designed CT low-pass DSM (a) Block diagram (b) Designed parameter values

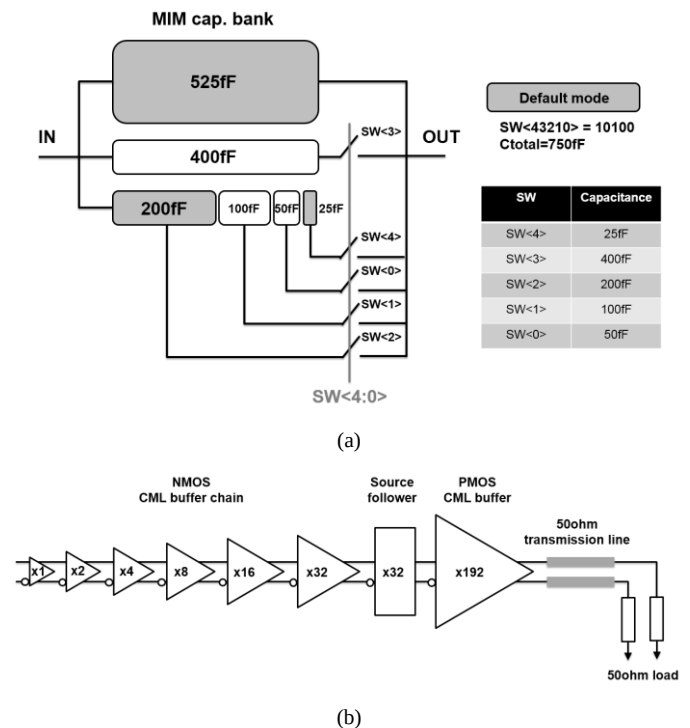


Figure 7. Circuit diagram of the capacitor banks for C1, C2 and C3 and the designed CML buffer

The simulation results with the parasitic extracted view of the modulator circuit are shown in Figure 8. The simulated peak SNDR was 49.4 dB for the bandwidth of 20 MHz. In the case of the 10 MHz bandwidth, the SQNR is approximately 3 dB higher than the peak value. In the spectrum of the peak SQNR case in Figure 8 (b), a noise notch was observed as expected. The high-amplitude tone near 3.6 MHz is the 3rd order non-linearity of the input sinusoid signal at 1.215 MHz. The final design results are summarized in Table 2.

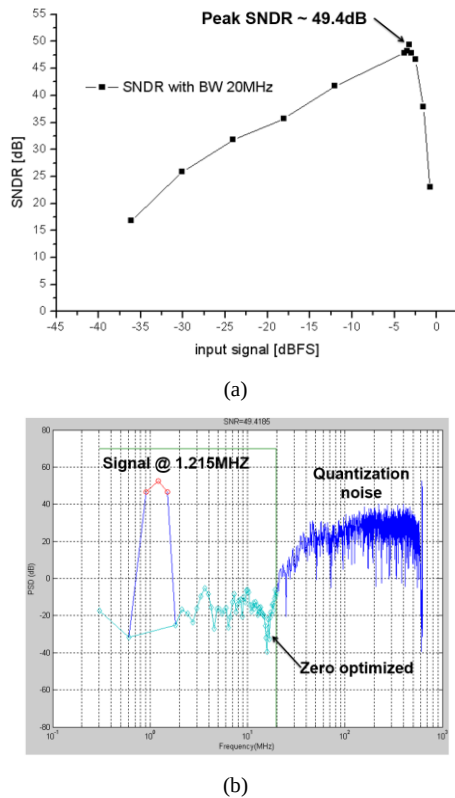


Figure 8. Post-layout simulation results: (a) SNDR vs input signal level (b) spectrum of the peak SNDR case

TABLE 2. SUMMARY OF THE DESIGNED DSM CIRCUIT

Parameter	Value
Process	Standard CMOS 130 nm
Power supply	1.2 V
Power consumption	14.4 mW (excluding CML buffer)
Signal bandwidth	DC – 20 MHz
Sampling clock	622.08 MHz
OSR (Over Sampling Ratio)	15.55
Peak SNDR (Parasitic extracted view)	49.4 dB @ -3.4 dBFS (20 MHz BW)
Output level	2-level

IV. CONCLUSIONS

In this paper, detailed design results of the CT low-pass DSM circuit used to digitize the LTE signal at 10 MHz IF frequency in a digital DAS system using IFoF architecture is provided. From the post-layout simulation results, the designed DSM circuit shows SNDR up to 49.4 dB with a bandwidth of 20 MHz. By adopting the zero optimization

technique for the NTF in the designed DSM, a high stop-band rejection can be obtained.

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