

Data alignment for multi-channel high-speed interfaces using PRBS patterns

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Abstract— Multiple FPGAs are used for high speed and large amount of data transfer and also designed to implement DSP functions. The consecutive PRBS patterns are used for bit synchronization and data alignment between high-speed multi-channel interfaces of FPGAs.

Keywords— bit synchronization, data alignment, multi-channel I/O, PRBS patterns

I. INTRODUCTION

In high speed and large amount of data transfer systems such as the optical OFDM, multiple FPGAs are used for implementation of DSP functions. For implementation of the system, multi-channel high-speed I/O should be supported. Also, the bit synchronization scheme and the multi-channel data alignments are required [1-2].

In general, high-speed I/O systems have a function of bit synchronization and data alignments using such a 64B/66B encoding and decoding scheme [3]. However, additional 2bits are needed to find synchronization mark and it increases data transfer loads. To overcome this problem, we propose to use PRBS (Pseudo Random Binary Sequence) patterns to synchronize and align the multi-channels without additional data bits.

II. PRBS PATTERN CHARACTERISTICS

The consecutive PRBS patterns are not easy to synchronize bit by bit and align word data using only PRBS check logic. In this paper, PRBS patterns including the bit which indicates the location of synchronization point are generated in the transmitter. And the receiver detects the position of synchronization bit to find how many level shifts are calculated for bit synchronization and data alignment.

A. 64B/66B

In general, such as 64B/66B, added 2bits of overhead bit are needed in order to synchronize or align the data. However, there is a problem in that overhead is generated as a control signal for data transmission, thereby increasing the data transmission throughput. There is also a method of performing bit synchronization for each lane by using the fixed data pattern which includes a predetermined start pattern is transmitted, the receiver adjust the received data to synchronize and align. In this case, there is a disadvantage in

that it takes time to continuously transmit a predetermined pattern for training period.

B. PRBS Patterns

In general, the common PRBS patterns represent the polynomials are PRBS7, PRBS9, PRBS11, and so on. The PRBS has the maximum length of 2^k-1 sequences and k means the size of unique data in the sequence. The PRBS patterns are generated using linear feedback shift registers [4]. Therefore, the unique pattern is repeated with the maximum length and moves one bit in the most significant bit direction.

Depending on the channel characteristics, the signal transmission through the channel has a delay time of random value due to various factors such as thermal noise and interference of other channels. Especially, the difference in length between each lane occurring on the PCB induces the different latency between the transmission channels, so called as lane-to-lane skew [5]. Therefore, the arrival times at the receiver due to lane-to-lane skew are different, so that the received data should be aligned. However, even if different delay times occur, the PRBS patterns shifts through the channel. Therefore, it is not known whether or not the received PRBS pattern is delayed only by using the PRBS check logic. In order to synchronize and align data using consecutive PRBS, a new scheme is required.

C. PRBS Patterns with a special bit

In this paper, the transmitter sends continuous PRBS sequences having special bit to the receiver for synchronization and alignment. For example, a special bit is an error value in the transmitted PRBS sequence. In the receiver, the PRBS sequence with an error can be detected with PRBS check logic. Also, a bit shift occurs due to the noisy channel characteristics during transmission and the position of the error value is changed corresponding to the desired error position in transmitter.

For example, as shown in Figure 1, the PRBS patterns of from A, B, C' and D are transmitted and C' is expressed as the erroneous PRBS of the data pattern C to be transmitted correctly. The pattern including the error bit is transmitted with a delay time through the channel, and the data received at the receiver are from H, I, J' and K. The received PRBS patterns are the same order, but the sequence of the PRBS patterns have the different values due to the delay time. The data pattern J' has an error bit in a position different from the

data pattern C' . The delay time through the channel can be measured by calculating the difference between the error bit positions.

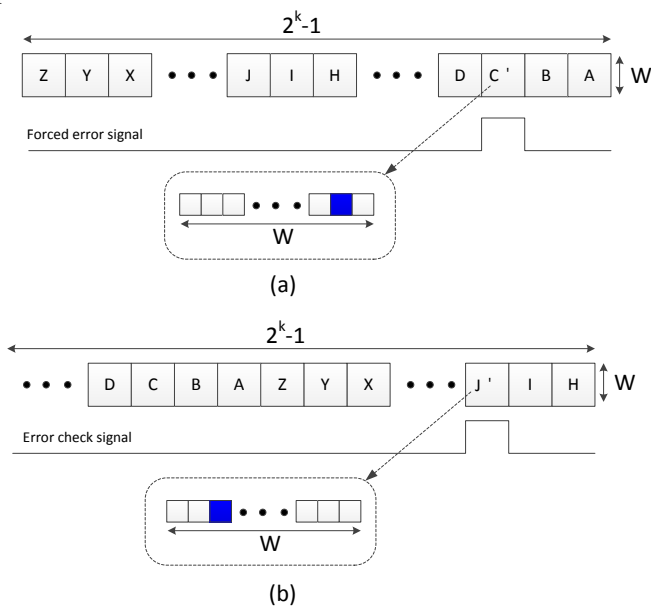


Figure 1. Example of PRBS pattern transmission with an error bit.

In the figure, the coloured rectangle in dotted box indicates that the error bit position in data width of W is changed through transmission. For example, assuming that the 8bit data pattern to be transmitted is “10110100”, the data pattern including the error bit is “10110000” from the left and the received data pattern is “011000011”. It is assumed that an erroneous PRBS pattern is received. In this case, the error bit is generated from the sixth from the left and if it is normally received without the channel delay time, the error bit is generated at the sixth bit, so that a 1 bit delay time has occurred in the channel.

III. OVERALL SYSTEMS AND SIMULATION RESULTS

The Figure 2 shows the Overall systems of multi-channel I/O with PRBS pattern generator and checker. It consists of transmitter and receiver. The transmitter has PRBS generator in each lane and the receiver has PRBS checker and aligner.

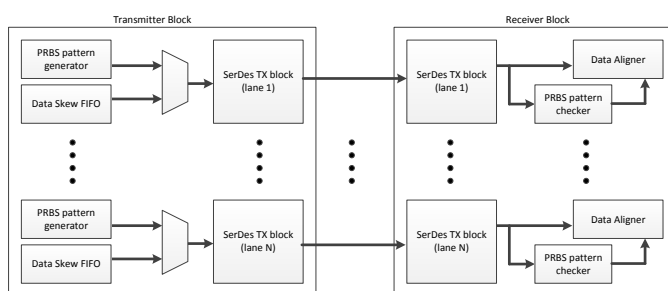


Figure 2. Overall block of multi-channel interfaces

The transmitter block consists of a PRBS generator, a forced error generator, a selector and SerDes transmit block, as shown in Figure 3. As described above, the PRBS generator

generates a data width W in accordance with a selected polynomial and a maximum length sequence in which a data value having a value of 2^k-1 is repeated. The forced error generator sets the value to ‘1’ so that an error occurs at a predetermined bit position within the data width W and sets the remaining bits to ‘0’ so that an error does not occur. When the PRBS pattern generated by the PRBS generator and the bit value of ‘1’ corresponding to the error occurrence position set by the forced error generator are XORed by the selector, the corresponding bit position in the PRBS pattern is generated to have an error. However, the forced error generator and the selector operate only for one pattern in which an error is desired to be generated in the process of PRBS pattern transmission.

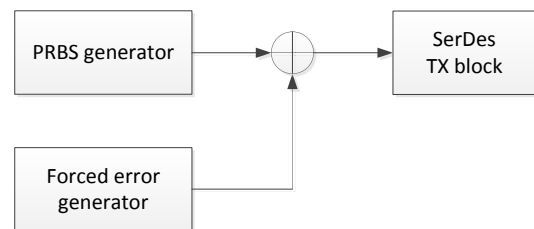


Figure 3. Detailed block diagram of transmitter

As shown in Figure 4, the receiver block consists of a SerDes receiver block, a PRBS checker, a forced error checker, a bit shifter and data aligner. The data received at the SerDes receiver block is determined whether an error has occurred in the received PRBS pattern using a PRBS checker. If an error occurs, the PRBS checker indicates that the PRBS pattern including the error is transmitted from the transmitter and notifies the forced error checker that an error has occurred. The error pulse signal from the PRBS checker is transmitted to the forced error checker in that the pattern with an error is found. Since the position of the error bit to be included in the PRBS pattern at the transmitter has already been determined, it is assumed that the receiver also knows the position of the error bit. The forced error checker that knows the position information of the determined error bit finds the error occurrence position in the received PRBS patterns and calculates the position of the transmitted error bit and the position of the determined error bit. It outputs the difference value of the calculated bit position to the bit shifter. The bit shifter moves the bit stream of the PRBS data pattern by the calculated bit difference to compensate the delay time so that the PRBS data pattern is correctly recovered. In each lane of the receiver, the error occurrence pulse signal or error bit position value from the bit shifter is transmitted to the word aligner together with the received data. The word aligner performs data skew alignment using the error signal and data pattern. If the error occurrence pulse signal is received from each lane, it is aligned with the lane corresponding to the data pattern at the latest error signal point. Also, if the error bit position value is received from each lane, it is aligned based on the largest position value. The word aligner may include a word FIFO. Accordingly, the data pattern for each lane received from the receiving block is stored and word

alignment is possible to read the stored data from the FIFO at the latest time of error pulse signals or based on largest position values from every lane.

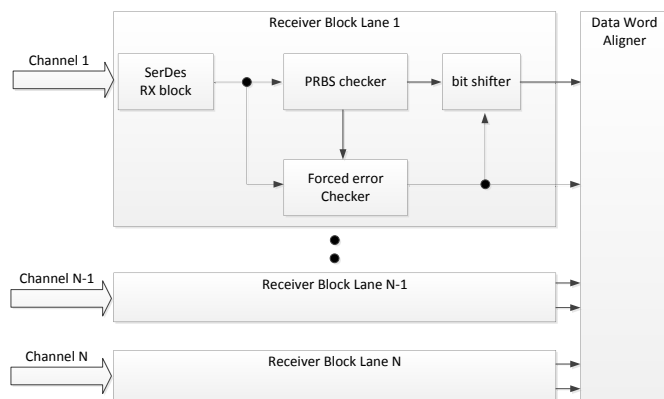


Figure 4. Detailed block diagram of receiver

Figure 5 shows HDL simulation results of the proposed transmitter and receiver with PRBS patterns. In the simulations, the transmitter generates the PRBS with an error in the least significant bit. In this paper, Xilinx FPGA is used, and the MGT (Multi Gigabit Transceiver) provided by Xilinx has a function to shift the received data manually by one bit with control signal. Thus, the three pulse signals mean that they are three bit shifted as shown in (1) of the figure. In order to confirm whether the bit synchronization normally operates, the fixed data pattern of 64bits hexa values such as “aaaaaaa55555555” is transmitted as illustrated in (2) of the figure. Finally, when the read signal of FIFO is activated with the latest error signal, the FIFO’s output data is validated and matched as shown in (3) of the figure.

IV. CONCLUSIONS

In conclusion, the method for bit synchronization and word data alignment using PRBS patterns are proposed and can easily perform multi-channel PRBS pattern transmission without data overhead. The proposed scheme is implemented and simulated with HDL in Xilinx FPGA environments. In the future, the proposed method will be applied to implement the actual multiple FPGAs system.

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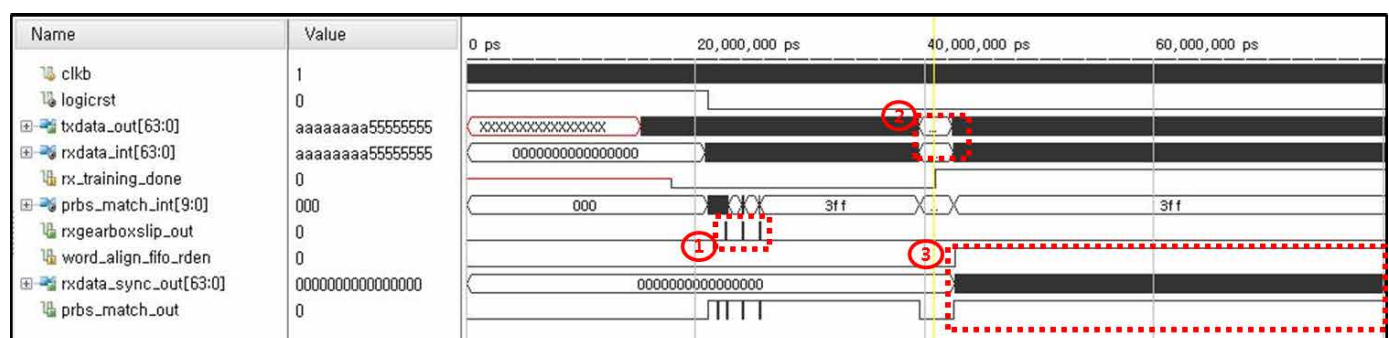


Figure 5. HDL simulation results