

1.8V-to-1.0V CMOS 65 nm MIPI RFFE Interface Circuit for Millimeter-wave Beamforming Array

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Abstract— A 1.8V MIPI RF front-end (RFFE) circuit for a slave with a 1.0V supply is designed using a CMOS 65 nm process as a control block for a millimeter-wave beamforming array. It is consisted of a MIPI RFFE slave logic, power-on-reset (PoR), SCLK receiver, and SDATA transceiver to support the MIPI RFFE master-slave interface with MIPI RFFE bus. According to simulation results, the designed MIPI RFFE interface circuit provides rise and fall time of less than 3.3 ns with a 26 pF load (one master-eight slave configuration) at the transmission rate of 26 MHz, satisfying the requirement of 6.5 ns in the MIPI RFFE specification version 1.10.

Keywords— beamforming, 5G, mobile communication, MIPI, RFFE, PoR, SCLK, SDATA

I. INTRODUCTION

The International Telecommunication Union (ITU) has approved IMT-2020 as a recommendation for fifth-generation (5G) mobile communication to provide standard specifications. More importantly, 3GPP, the most promising standardization organization for industries, recently completed release 15 where the standard specifications of phase 1 of the 5G system are described. One of the most noticeable contents in the 3GPP release 15 is that, unlike the previous specifications for mobile communication systems such as LTE (<6 GHz), the millimeter-wave band is considered for a mobile communication carrier frequency. In this effort, numerous researches and developments of circuits and systems for high-frequency and high-capacity communications have been carried out in both wired and wireless areas [1-8].

In the present paper, as shown in Figure 1, a MIPI RFFE slave circuit including a slave logic and interface circuits for a millimeter-wave beamforming array for 5G mobile communication is designed using a CMOS 65 nm process, and the simulation results are provided. A beamforming array is perceived as a key component making such high-carrier-frequency communication possible. As a means of controlling the gain and phase of transmit/receive signals in the beamforming array, MIPI RFFE is one of the best options because MIPI RFFE interface is prevalent in cellular RF front-end modules, simplifying the overall control scheme of a 5G front-end module [9,10].

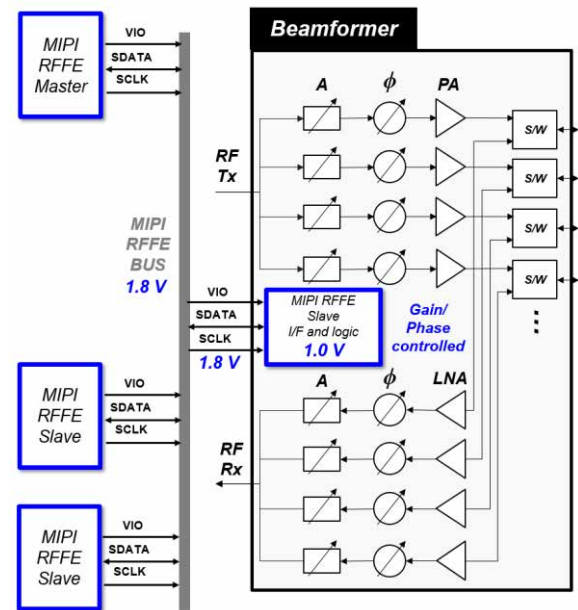


Figure 1. Block diagram of MIPI RFFE interface in 5G mmWave beamforming array

II. OVERALL STRUCTURE OF MIPI RFFE INTERFACE

Figure 2 shows the overall block diagram of a designed MIPI RFFE interface circuit. In the master-slave configuration, a MIPI RFFE master controls multiple slaves, and a MIPI bus with VIO, SDATA and SCLK is shared among the master and slaves so as to communicate from each other.

A PoR provides a low-active signal for a relatively long time period (RESET) to all the other MIPI RFFE circuits, to ensure the circuits to be fully initialized after a VIO is applied.

In transmit mode with a 'low-state' READ, a bidirectional SDATA transceiver transmits a TXDATA digital signal from a 1.0V RFFE slave logic onto the 1.8V MIPI bus to be received by a MIPI RFFE master. This is because the voltage levels specified for the MIPI bus are 1.2 V and 1.8 V according to the MIPI RFFE specification, and the 1.8 V level is selected for the control interface of the beamforming array. In receive mode by a 'high-state' READ, SDATA on the RFFE bus is received,

level-converted from 1.8 V to 1.0 V, and delivered to the slave digital logic as RXDATA.

The MIPI master also provides a clock signal, SCLK, for the aforementioned operation. Typically, a hysteretic-comparator-based level converter is used to receive the SCLK on the bus and converted into CLK as a clock signal for the entire interface circuit.

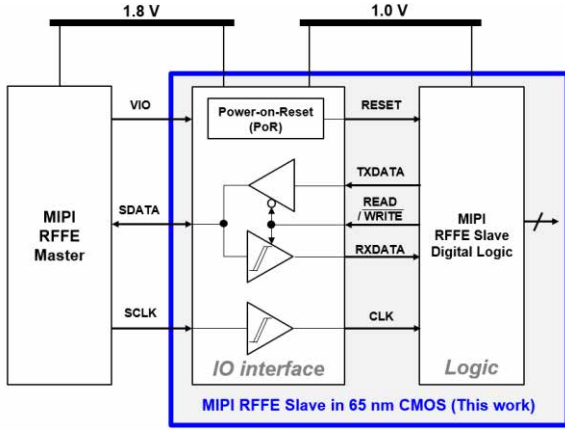


Figure 2. Overall structure of the designed MIPI RFFE interface

III. CIRCUIT DESIGN OF MIPI RFFE INTERFACE

The detailed design results of the three circuit blocks of PoR, bidirectional SDATA transceiver, and SCLK receiver for MIPI RFFE slave are described in this section.

A. Power-on-Reset

To provide a long active-low pulse in time for initialization of the designed MIPI RFFE circuits, a cascade of current mirrors, a large capacitor, and a Schmitt trigger are exploited in PoR, as shown in Figure 3. By reducing the sizes of current mirrors towards the delay capacitor (M9), a considerably small amount of current of 2 nA can be generated and injected into the metal-oxide-metal (MoM) capacitor with a capacitance of 20 pF. As a result, the voltage at the positive node of the delay capacitor (M9) increases slowly with the small current and the large capacitor. This slowly-increasing voltage is then fed into the input of the Schmitt trigger, and finally converted into a digital signal to be used as the long initialization pulse.

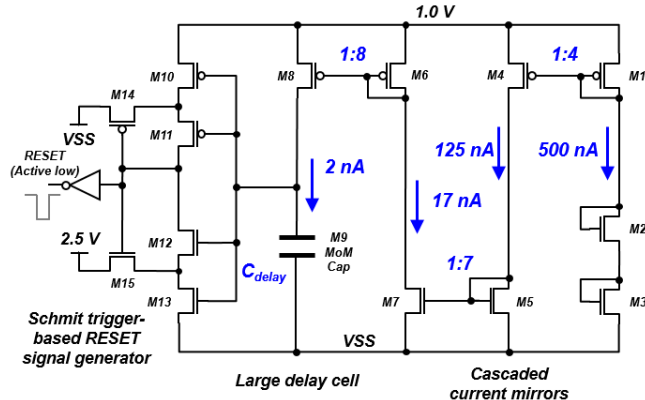


Figure 3. Designed circuit of a power-on-reset to provide an initialize signal for MIPI RFFE slave

The transient simulation result of the designed PoR circuit is depicted in Figure 4. The time period of the 'low-active' RESET is approximately 3.8 ms. As shown in Figure 4, with the Schmitt trigger, a longer 'active-low' RESET signal can be obtained with the hysteretic characteristic of the circuit.

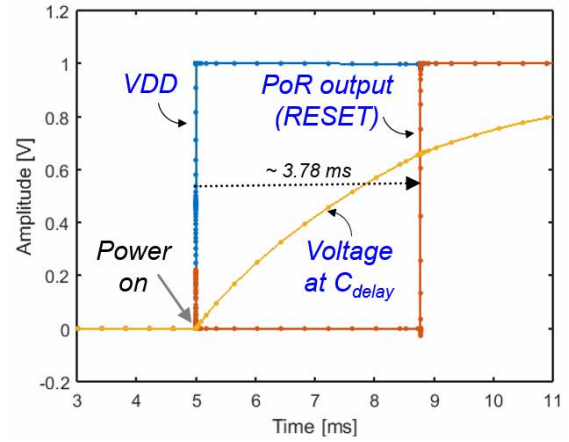


Figure 4. Simulated transient result of the designed PoR circuit

B. SCLK Receiver

Figure 5 shows the circuit diagram of the designed SCLK receiver. A hysteretic comparator-based level converter is used in the clock receiver to reconstruct a cleaner clock signal because SCLK in the MIPI bus is shared with other slaves and therefore is vulnerable to external noise.

A level converting operation from 1.8 V to 1.0 V is also conducted in the receiver to properly and securely drive the slave logic circuits.

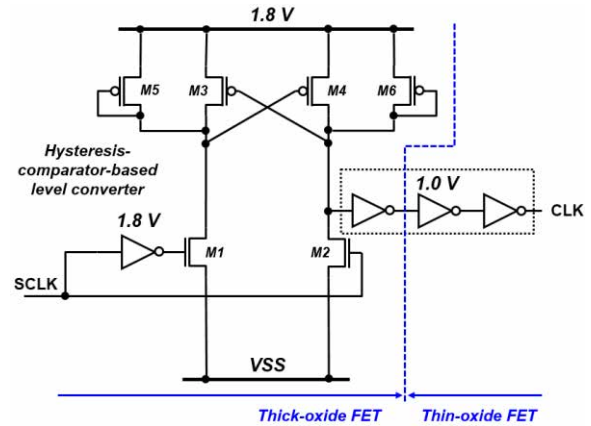


Figure 5. Designed circuit of an SCLK receiver to regenerate a clock signal for the MIPI RFFE slave logic

C. SDATA transceiver

The block diagram of the designed SDATA transceiver is illustrated in Figure 6(a).

The SDATA line in the RFFE bus is shared and connected to the output of the SDATA transmitter and the input of the SDATA receiver. The transmit and receive mode is controlled by the 'READ' signal with 'high-state' and 'low-state' for 'receive' and 'transmit' modes, respectively.

The circuit diagrams of the designed SDATA transmitter and receiver are shown in Figure 6(b) and (c), respectively. Because SDATA in the bus is shared among the transmitter and receiver, the final stage of the transmitter and the input stage of the receiver are designed for a tri-state operation (high-state, low-state, and high impedance), and the 'READ' signal determines the states.

The SDATA transmitter consists of a 1.0 V-to-1.8 V level converter and an inverter chain with the tri-state operation. To properly drive a high capacitive load by up to eight MIPI RFFE slaves connected to the same bus, the transistor sizes of the final stage must be thoroughly designed to satisfy the rise and fall time requirements of < 6.5 ns by the MIPI RFFE specification version 1.10 [9,10].

The SDATA receiver is almost the same as the SCLK receiver except for the tri-state operation. By adding only two more transistors of M7 and M8 to the SCLK receiver, the tri-state operation can be easily obtained, simplifying the circuit structure and reducing the power consumption.

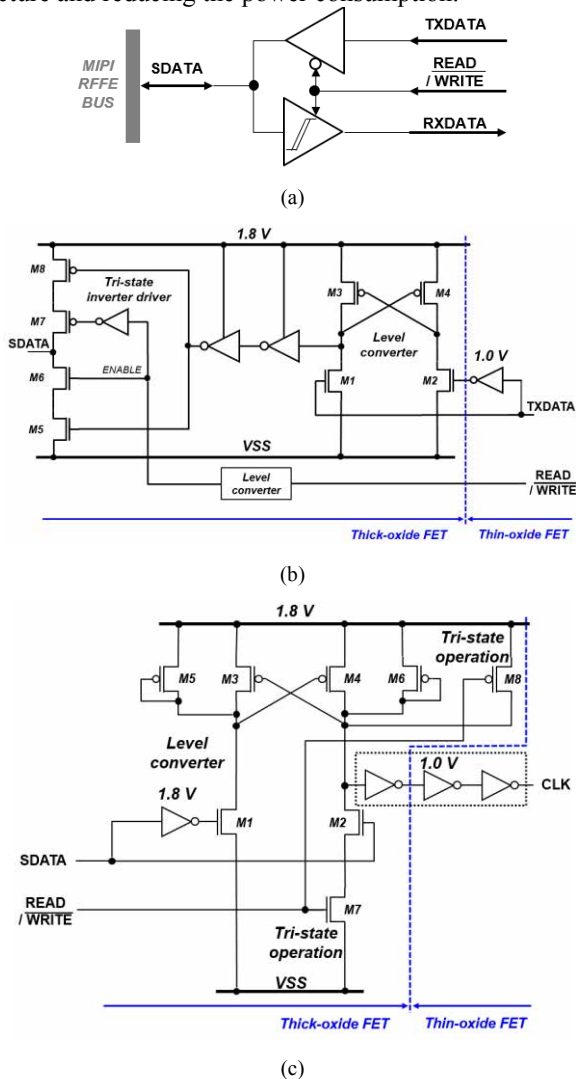


Figure 6. (a) Block diagram of the designed SDATA transceiver, (b) Circuit diagram of the designed SDATA transmitter, (c) Circuit diagram of the designed SDATA receiver

The simulation results of the designed SDATA transceiver are depicted in Figure 7(a) for transmit mode and Figure 7(b) for receive mode with a capacitive load of 26 pF connected to the SDATA bus.

According to the simulation results, the propagation delay from TXDATA to SDATA in transmit mode is less than 1.9 ns, and the rise and fall time of the SDATA pulse is less than 3.3 ns, satisfying the requirement of < 6.5 ns by the specification. In receive mode, the simulated propagation delay from SDATA to RXDATA is approximately 0.65 ns.

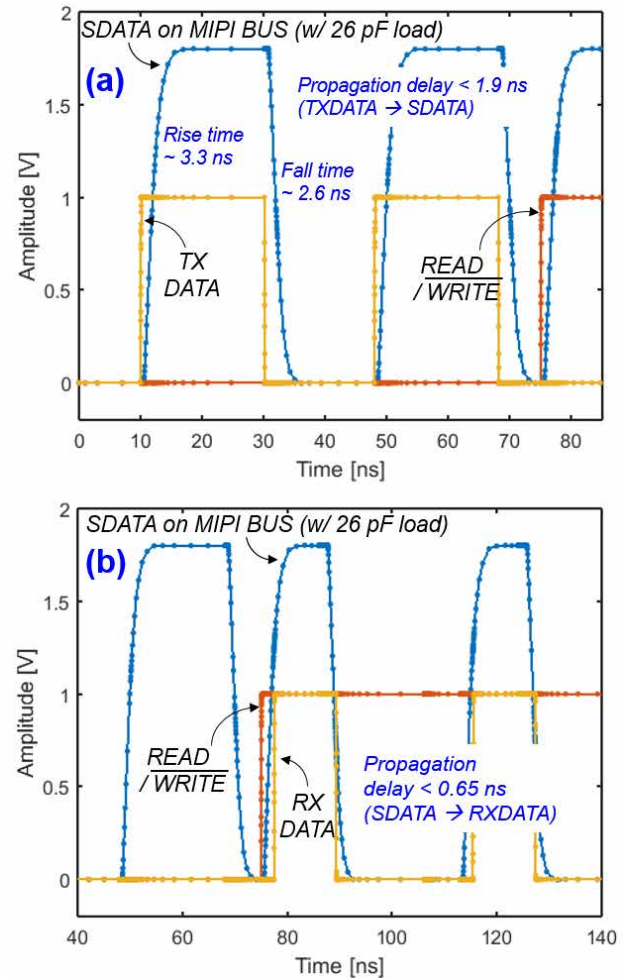


Figure 7. Transient simulation results: (a) Designed SDATA transmitter (b) Designed SDATA receiver

D. Layout of the Designed MIPI RFFE Interface Circuit

The layout of the designed MIPI RFFE circuit is shown in Figure 8. The size of the whole circuit layout is $340\mu\text{m} \times 130\mu\text{m}$ using a CMOS 65 nm process. The layout size of the RFFE slave logic, the SCLK receiver and the SDATA transceiver is $180\mu\text{m} \times 130\mu\text{m}$.

Because the size of the PoR in Figure 8 is significantly dependent on the size of the delay capacitor, the capacitance value of the capacitor can be reduced with a shorter 'RESET' signal.

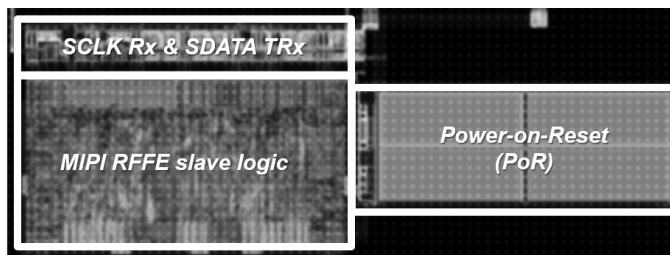


Figure 8. Layout of the designed MIPI RFFE interface circuit using a CMOS 65 nm process

IV. CONCLUSIONS

In this paper, the design and simulation results of a 1.8 V-to-1.0 V MIPI RFFE slave circuit using a CMOS 65 nm process satisfying MIPI RFFE specification version 1.10 are provided. The rise and fall transition time of SDATA clocking at 26 MHz in transmit mode is less than 3.3 ns with a highly capacitive load up to 26 pF for eight slaves. The simulated propagation delays of the SDATA transmitter and receiver are 1.9 ns and 0.65 ns, respectively. The layout size of the whole MIPI RFFE slave circuit is 340 μ m x 130 μ m (180 μ m x 130 μ m without PoR).

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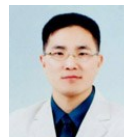
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