

The Research of Scheduling Algorithm Based on Time-Triggered Ethernet

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Abstract— This Time-triggered Ethernet (TTE) is a valid manner to ensure the timeliness, reliability and accuracy of time-triggered (TT) messages which make up for the shortcomings of traditional Ethernet. Satisfiability Modulo Theories (SMT) is the main theory to generate the traditional TTE schedule. However, the calculation time of SMT is too long when the number of time-triggered messages is large. To solve the problem, bin-packing algorithm is applied to the scheduling problem. This paper aims to optimize and improve the bin-packing algorithm including the packing rules and empty box design method based on the principle of the two-staged bin-packing algorithm. With the improved algorithm we proposed, it can ensure the feasibility and porosity of scheduling table. Additionally, it can also improve the transmission performance of event-triggered (ET) messages without affecting TT messages transmission. The simulation results show that the improved algorithm reduces the latency of the ET messages and greatly shortens the calculation time of the scheduling algorithm.

Keywords— Time-Triggered Ethernet; Schedule; Bin-packing algorithm; Porosity

I. INTRODUCTION

With the rapid development of information technology and driven by strong demand, Airborne avionics network technology is playing an increasingly prominent role in national defense construction. The traditional low-speed airborne bus technology has been unable to meet the development needs of the future avionics system, and is gradually evolving toward the direction of high-speed switching avionics network technology.

Time-Triggered Ethernet (TTE), which could satisfied well of distributed avionics system communication, has strong real-time property and certainty, and raises wide concern in field of aerospace electronics [1]. Time Triggered Ethernet is a real-time network technology based on Time Triggered protocol developed on the basis of standard Ethernet. Time-Triggered Ethernet, which supports both Time Triggered (TT) services and Event Triggered (ET) services based on the IEEE 802.3 Ethernet standard and compliant with ARINC664p7 [2]. TTE combines the real-time, deterministic and fault-tolerant capabilities of time-triggered transmission with the flexibility and dynamics of traditional Ethernet “best-effort transmission” to support applications with mixed-criticality

requirements [3][4]. The architecture of TTE is shown in the Figure 1.

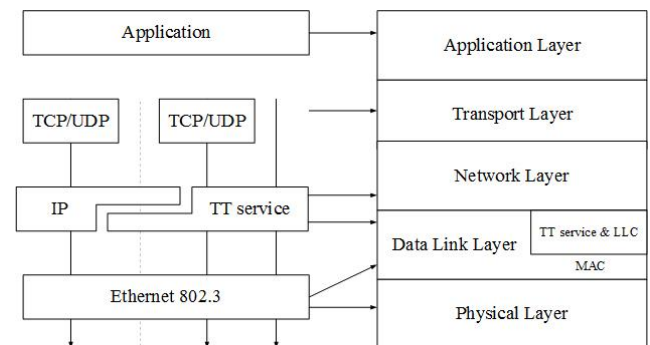


Figure 1. Time-triggered Ethernet architecture

The SAE AS6802 standard has an accurate definition of TTE[5]. TTE supports the transmission of three kinds of messages at the same time, they are time-triggered message (TTM), Rate-Constrained Message (RCM) and Best-Effort Message (BEM). The transmission of TTM is strictly controlled by a pre-designed schedule. RCM and BEM are event-triggered messages. They have lower priority than TTM and can only be transmitted during the idle time period of the TTM, without any impact on the TTM.

TTM is known before transmission and they have strict requirement of time limitation, so TTM need to be arranged in advance. Therefore, the schedule generation strategy is very important for the communication performance of TTE. The traditional method is to use the SMT solver to generate the schedule. The SMT solver generates a feasible schedule by searching the Boolean variables associated with the scheduling propositions [6]. This method is low in optimization and high in algorithm complexity. When the number of TTMs is large, the calculation time of the SMT solver will increase exponentially [7]. Later, a strategy of combining the bin-packing problem with the scheduling has been proposed [8]. This method can effectively reduce the complexity of the algorithm and reduce the occupation of the time slice by TTM, so that ET messages have more time slices for transmission. However, this algorithm will cause the TTMs to accumulate excessively, thus seriously affecting the available time distribution of ET messages. Therefore, it has

an impact on the delay and jitter performance of the TTE. Not only that, but the algorithm also needs to use heuristic algorithm for search optimization [9], so the calculation time is still relatively long.

This paper proposes a new improved solution on this basis of optimizing the packing algorithm, making it more suitable for TTE scheduling problem. The improved algorithm performs pre-processing on TTM before scheduling, eliminating the step of search optimization. And adding porosity to the schedule, thereby improving the delay and jitter performance of the ET messages. Therefore, the improved algorithm has lower complexity and better performance, which is also proved in the simulation results.

The remainders of this paper are organized as follows: This paper continues in Section II with the introduction of the system model. In Section III, we describes The Bin-packing schedule algorithm. Then, our optimization algorithm is proposed in Section IV. Finally, we conclude this paper in Section VI.

II. SYSTEM MODEL

Suppose that the TTE network topology is shown in Figure 2. There are 22 terminal nodes and 2 switches in network, which focuses on two-way traffic transmission and virtual links. The real thick lines represent the actual physical links, and the thin arrows represent the transmission links of the message frames, which are directional and contain the information of the source and destination nodes.

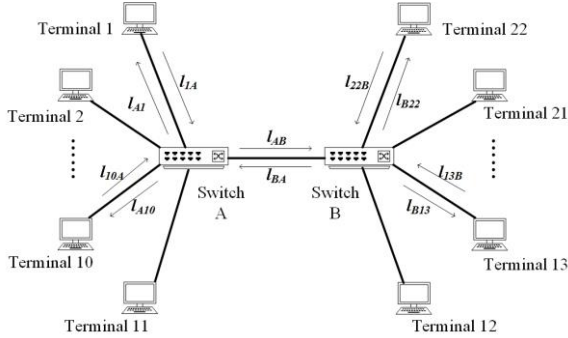


Figure 2. Time-triggered Ethernet topology

If a TTM's source node is n_i and its destination node is n_j , then define its data link as $l_{ij} = [n_i, n_j]$. The link path is defined as follows:

$$P_{ij} = l_{in} + l_{nm} + \dots + l_{mj} \quad (1)$$

Therefore, the link path from terminal 3 to terminal 22 can be expressed as: $P_{322} = l_{3a} + l_{ab} + l_{b22}$. The virtual link (VL) is made up of all link paths P_{ij} sets, which can be defined as follows:

$$VL = \bigcup P_{ij} \quad (2)$$

When all data links of two link paths P_n and P_m do not cross, then the two TTMs can be transmitted synchronously

without conflict. Therefore, for the network topology shown in Figure 2, the network topology can be divided into three regions, and TTMs in different regions can be transmitted synchronously. The set of all nodes in the network architecture is defined as *Nodes*, which is divided into several regions according to the network topology. The set of *Nodes* in the region is defined as $Zone_i (i = 1, 2, \dots, N)$. It satisfies the following constraints:

$$\begin{cases} Zone_i = Nodes \\ Zone_i \cap Zone_j = \emptyset \\ N = \bigcup Zone_i \end{cases} \quad (3)$$

According to the source node and destination node of TTM and the network structure, we can get the set of nodes that the TT frame travels through, which can be expressed as $n_{az} = n_a, n_b, \dots, n_z$, its subscript symbol indicates the mark of nodes passed through. Therefore, the region of the TTM can be known by comparing the path nodes and the region nodes. So a two-dimensional variable $syn_{ij} = \{0, 1\}$ is defined as the attribute parameters of TTMs. When the variable is 0, the frame i and the frame j cannot be transmitted synchronously; when the variable is 1, the frames can be transmitted synchronously. Its constraints are defined as follows:

$$\begin{aligned} & \text{if } \begin{cases} Occupy_a = \{i \mid n_a \cap Zone_i \neq \emptyset\} \\ Occupy_a \cap Occupy_b \neq \emptyset \end{cases} \quad syn_{ab} = 0 \\ & \text{if } \begin{cases} Occupy_a = \{i \mid n_a \cap Zone_i \neq \emptyset\} \\ Occupy_a \cap Occupy_b = \emptyset \end{cases} \quad syn_{ab} = 1 \end{aligned} \quad (4)$$

III. SCHEDULE GENERATION ALGORITHM

The TTE schedule specifies when to send, forward, and receive the TTM to ensure the timeliness of the TTM.

The TT frame is defined as:

$$tt.frame = \{id, period, length, source, sink\} \quad (5)$$

The TT frames have different *periods* and *lengths*. So in order to ensure that the TTE can work continuously, we can find a long period. In this period, all TTMs can complete at least one cycle. This period is also the length of the schedule. The TTE system will repeat the scheduling according to the schedule to ensure the correct transmission of the TTM.

In SAE AS6802, Cluster Period (CP) is defined as the period for all TT frames. Cluster Period is usually the least common multiple (LCM) of all *periods*, or an integer multiple of the LCM.

$$CP = n \cdot [tt.period_1, tt.period_2, \dots] \quad n \in N_+ \quad (6)$$

The problem can be abstracted to load items into an empty box, where TTM is the "item" and Cluster Period is the "empty box".

First, we abstract TTM into two-dimensional items [10]. If the period of a TTM is short, it means that it will repeat more

times in the schedule, which means it will take more time resources. Similarly, when the length of a TTM is long, it means that more time is used for transmission. So we define the length and width of the item as follows:

$$width_{id} = tt.length_{id} \quad (7)$$

$$length_{id} = CP / tt.period_{id} \quad (8)$$

Then, design the empty box similarly.

$$width_{box} = MP = (tt.period_1, tt.period_2, \dots) \quad (9)$$

$$length_{box} = CP / width_{box} \quad (10)$$

The bin-packing algorithm ensures that there is no conflict in TTM, and time resources is utilized efficiently, respectively.

There is a example running process of the bin-packing schedule generation algorithm is shown in the Figure 3. The information of TTM is shown in the Table I. Assume that all TTMs cannot be transmitted synchronously. Figure 3(a) shows the packing result, Figure 3(b) shows the result of dividing the TTMs by period, and Figure 3(c) shows the schedule corresponding to the packing result. For two TT frames that can be transmitted synchronously, it means that one item can regard the space occupied by the other one as available during the packing, thus improving the utilization of time resources and link resources. Assuming E and B can be transmitted synchronously, then the result is shown in Figure 3(d).

TABLE 1. THE INFORMATION OF TTM

	A	B	C	D	E
period(ms)	1	2	2	4	8
length(bit)	10	20	25	10	25

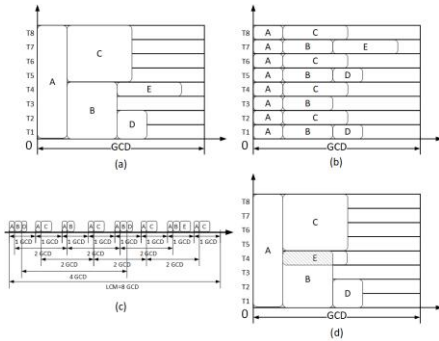


Figure 3. Bin-packing scheduling algorithm process

IV. IMPROVED ALGORITHM

According to the introduction of the packing schedule generation algorithm in the previous chapter, we can know that in the existing related research [8], the optimization of the algorithm is to make the TTM occupy the least number of time slices. Although this will reduce the waste of time resources, this will cause excessive accumulation of TTM, which will increase the delay and jitter of subsequent ET messages.

This paper solves this problem by optimizing the packing algorithm. Under the premise of ensuring the timeliness and

conflict-free for TTM, the improved algorithm makes transmission delay of the subsequent ET messages lower, the performance better and the system more stable. Not only that, but the improved algorithm has lower complexity and the calculation time consumption has a significant decline.

A. The two-staged bin-packing algorithm

The two-staged packing algorithm is divided into two stages in the process of algorithm execution [11]:

- In the first stage, the items waiting for packing are arranged and processed according to a certain rule (combination or initialization), and the processed items are regarded as a new item to be packed.
- In the second stage, the new items are loaded in the boxes according to the packing rules.

IH packing algorithm is one of the two-staged packing algorithms [12].

B. The improved algorithm

Title On this basis, in order to ensure the porosity of TT scheduling, we divide the box into multiple layers. According to the idea of two-staged packing algorithm, the packing scheduling algorithm was divided into two stages.

The first stage, determine the region of the TTM. According to the network topology shown in Figure 2, the TTMs can be divided into three regions: A, B and AB.

Then processing the TTM. Because most of TTMs are short, so we group them according to the length of the TTMs. The grouping is defined as follows:

$$group(tt_{id}) = \text{int} \left(\frac{tt.length}{tt_{id}.length} \right) \quad (11)$$

If $group(tt_{id}) = 0$ means frames are longer than the average length. This group of TT frames will not stack with others. If $group(tt_{id}) = 1$ means the frames length is slightly smaller than the average length, and this group of TT frames will not stack with others either. If $group(tt_{id}) = n$ ($n \in N_+$) means the TT frames in this group are $1/n$ of average length, then sort the TT frames in the group according to their period. Then TT frames are bound to one block in order. The size of blocks is as follow:

$$height_{block} = \sum h(tt_{id}) \quad (12)$$

$$width_{block} = \max(w(tt_{id})) \quad (13)$$

Finally, we combine the blocks in region A and region B. Since the messages in region A and region B can be transmitted synchronously, the two blocks can overlap during the packing. After the blocks are sorted by size, select two blocks from each regions and combine them into one block.

The second stage, packing the blocks. Take out one block from the groups at a time for packing. The probability that each group is selected is proportional to the number of remaining blocks. This can ensure an even distribution of the different groups. The selected block is placed in the lower left corner of the layer box. If this layer is filled, then start the next

layer of box. Repeat this operation until all the blocks are placed in the box.

V. PERFORMANCE EVALUATIONS AND DISCUSSIONS

In order to evaluate the performance improvement of the improved algorithm, we build a simulation platform based on the above assumptions. The TTE network topology is as shown in Figure 2, which consists of two switches and each connected to 11 terminal nodes. Suppose the switch can only process one message in one time slot, so the messages in region A and region B can be transmitted synchronously. According to the two versions of the bin-packing scheduling algorithm, the packing results are shown in Figure 4 and Figure 5 separately. As can be seen from the figures, the improved algorithm schedules the TTM in layers and increases the porosity of the scheduling table, which can reduce the probability of ET message queuing. Therefore, the queuing delay of the ET message is reduced, and the performance of the network is improved.

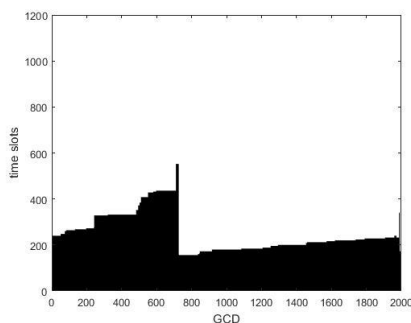


Figure 4. Bin-packing result of original algorithm.

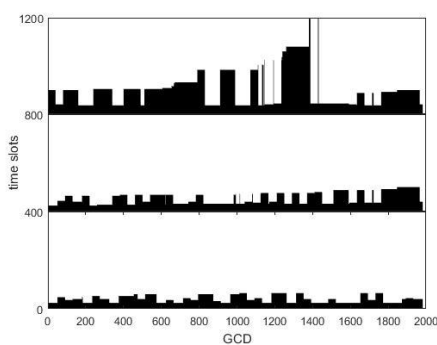


Figure 5. Bin-packing result of improved algorithm

Then, we build the communication environment of TTE, and control the transmission of TTM by schedules obtained by traditional bin-packing scheduling algorithm and improved version algorithm. Then calculates the delay performance of ET messages in the network. Figure 6 shows the delay performance curve of ET messages of traditional algorithm and improved algorithm when the number of TTMs changes. It can be seen from the figure that as the number of TTMs increases, so does the latency of the network. This is because the number of TTMs increases and more time resources are needed to service the TTM, so the remaining time resources

for serving the ET messages are reduced, resulting in an increase in latency. And the improved algorithm can significantly improve the delay performance of ET messages. Therefore, increase porosity of the TT schedule will reduce the queuing of ET messages. Therefore, the delay and jitter performance of the communication system are enhanced.

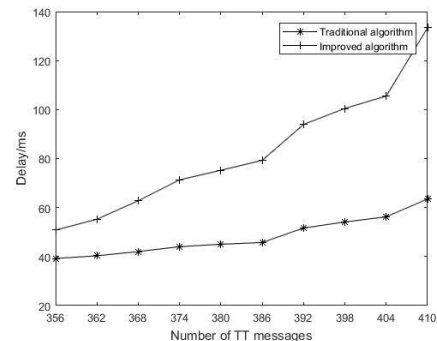


Figure 6. Delay performance comparison of two algorithms.

Figure 7 shows the calculating time comparison between the traditional algorithm and improved algorithm. As the number of TT messages increases gradually, the calculating time of both algorithms increases. However, the calculating time of the improved algorithm is significantly reduced compared with the traditional algorithm. The performance optimization of message preprocessing is demonstrated. The complexity is greatly reduced on the premise of guaranteeing the performance of the algorithm, so that the application of the algorithm to online scheduling can be considered.

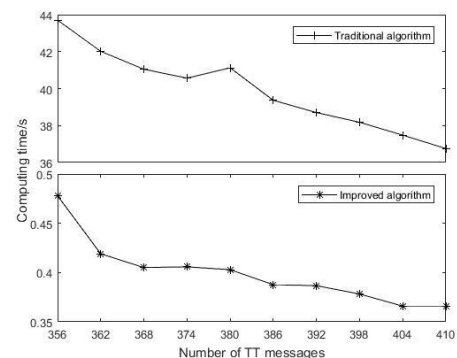


Figure 7. Computation time comparison of two algorithms

VI. CONCLUSIONS

In order to improve the performance of time-triggered Ethernet, this paper proposes an improved algorithm for generating schedule. The two-stages bin-packing algorithm is applied in the scheduling problem. The simulation results show that the new improved algorithm achieves a better delay and jitter performance on ET messages transmission with lower complexity. The average delay and jitter of the improved algorithm are significantly reduced, and the algorithm calculating time is also greatly reduced, providing a

more reliable, stable and flexible communication environment for time-triggered Ethernet.

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REFERENCES

- [1] A. Starke, D. Kumar, M. Ford et al, “A test bed study of network determinism for heterogeneous traffic using time-triggered ethernet,” MILCOM 2017 - 2017 IEEE Military Communications Conference (MILCOM), pp. 611 - 616, 2017.
- [2] 802.3-2012 - IEEE Standard for Ethernet - Section 1[J]. 2012:1-0.
- [3] Kopetz H. The Time-Triggered Architecture[C]// International Symposium on Object-Oriented Real-Time Distributed Computing. IEEE Xplore, 1998:22-29.
- [4] TTTech. Time-Triggered Protocol, High Level Specification Document. Vienna, Austria, D-032-S-10-28 Available at <http://www.ttech.com>
- [5] SAE Technical Standard.SAE AS6802[S]. SAE International.2011-11
- [6] Schröder C, Krenz-Bäh R, Murshed A, et al. Computing optimal communication schedules for time-triggered networks using an SMT solver[C]// IEEE International Symposium on Industrial Embedded Systems. IEEE, 2016.
- [7] Craciunas S S, Oliver R S. SMT-based Task- and Network-level Static Schedule Generation for Time-Triggered Networked Systems[C]// International Conference on Real-Time Networks and Systems. 2014:45-54.
- [8] Li B, Wang Y. Hybrid-GA based static schedule generation for time-triggered ethernet[C]// IEEE International Conference on Communication Software and Networks. IEEE, 2016:423-427.
- [9] Pop P, Eles P, Peng Z. Schedulability-driven communication synthesis for time triggered embedded systems[J]. Real-Time Systems, 2004, 26(3):297-325.
- [10] Huang J, Blech J O, Raabe A, et al. Static scheduling of a Time-Triggered Network-on-Chip based on SMT solving[C]// Design, Automation & Test in Europe Conference & Exhibition. IEEE, 2012:509-514.
- [11] Zhu W, Oon W C, Lim A, et al. The six elements to block-building approaches for the single container loading problem[J]. Applied Intelligence, 2012, 37(3):431-445.
- [12] Lodi A, Martello S, Vigo D. Approximation algorithms for the oriented two-dimensional bin packing problem[J]. European Journal of Operational Research, 1999, 112(1):158-166.



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