

Chip Antenna with Vivaldi-Like Structure for W-Band Design

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Abstract— This paper proposes an application for a W-band chip antenna using the CMOS 180nm process. The chip size is 800 μm ×1200 μm , and it employs by Vivaldi-like antenna for design and performance analysis. The bandwidth of simulation is 99.3 - 114.8 GHz. The result of measurement shows that the reflection coefficient (S11) is 91.1 - 107.1 GHz. The antenna gain is simulated by high-frequency electromagnetic simulation software, which is about -5 dBi to -4 dBi, and the deepest resonance point is at 108 GHz, showing a gain of -4.6 dBi.

Keywords— Chip antenna, millimeter-wave, CMOS, fifth generation, W-band

I. INTRODUCTION

In current 5G communication technology, higher transmission speeds, lower latency, and increased network capacity are achieved primarily through the addition of frequency bands and enhanced spectral efficiency. The millimeter-wave frequency range, known for its wide bandwidth, offers excellent data transmission speeds, making it a crucial tool in the field of high-speed wireless communication [1]. Millimeter-wave antennas are suitable for miniaturized solutions due to their high frequency, allowing for a significant reduction in antenna size [2, 3]. Chip antennas, which are integrated into chips, offer a viable solution for miniaturization. They can be applied to various small electronic devices such as smartphones, wearable devices, and IoT devices [4, 5].

In CMOS processes, the distance between metal layers is typically short, which may result in lower gain and radiation efficiency. The fabrication process is also influenced by the silicon substrate, leading to interference and inefficient propagation of antenna radiation, thus causing a decrease in antenna gain [6, 7]. Previous literature has addressed these issues and proposed solutions. These techniques include using meander-line monopole antennas combined with packaging substrates to improve radiation efficiency and gain performance [8]. Another approach involves integrating square Split Ring Resonators (SRR) as parasitic couplers with the feed antenna to increase gain and improve impedance matching [9]. In reference [10], cavity-backed stacked patch antennas were added to chip antennas to improve radiation performance, frequency range and minimize loss. There are

also studies that incorporate metallic posts and embedded guiding structures to reduce unnecessary losses [11].

The antenna proposed in this paper adopts Vivaldi-like antenna. The V-shaped slot design of the Vivaldi antenna provides wide bandwidth and is directional. However, implementing a true V-shaped slot in a chip antenna faces limitations in manufacturing and size. A rectangular slot is used as an alternative solution to overcome these issues. The S11 of the proposed chip antenna is lower than the -10 dB standard, covering 99.3 to 114.8 GHz. The bandwidth percentage for this range is 14.08%. The antenna achieves a gain of approximately -4.5 dBi in this frequency range. The measured data shows a bandwidth ranging from 91.1 - 107.1 GHz, with a bandwidth percentage of 16.14%.

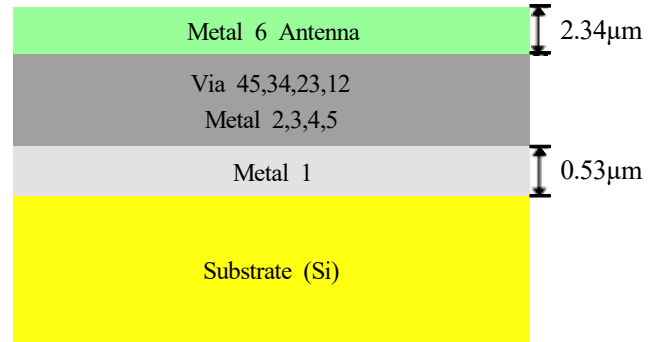


Figure 1. CMOS process stack diagram

II. ANTENNA DESIGN

The proposed chip antenna is developed using CMOS process. Fig. 1 shows the fabrication process, which includes six metallization layers. The thicknesses of metal 6 and metal 1 are 2.34 μm and 0.8 μm . Due to the dielectric constant and resistivity of the substrate, it is challenging to achieve high-gain chip antennas compared to other antennas [12, 13]. Therefore, the antenna is constructed by connecting Metal 6 and Metal 1, which helps reduce losses.

Fig. 2 and Table I illustrate the structure and parameters of the chip antenna, with a chip size of 800 μm ×1200 μm . In the antenna design, to mitigate the issues of low gain and efficiency caused by the CMOS process, a structure Vivaldi-like antenna is employed, using a rectangular slot as an

approximation of the V-shaped slot. The Vivaldi antenna structure can provide higher gain and directivity, enabling a longer communication range. Additionally, it can reduce scattering and effectively suppress interference sources [14]. Due to process density limitations, slot cutting was performed on the Metal 6 layer of the antenna. After simulation testing, it has been verified that there is almost no difference between the results with and without the slot cutting.

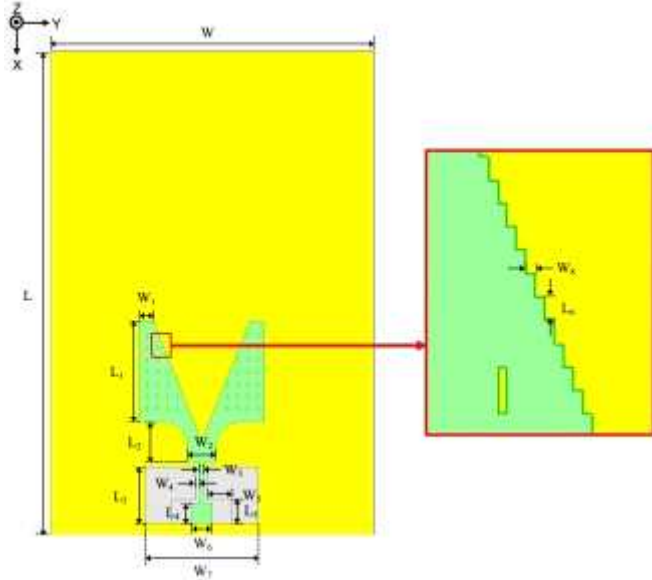


Figure 2. Geometric diagram of the Vivaldi-like antenna.

TABLE 1. ANTENNA ARCHITECTURE PARAMETERS

Parameter	Value(μm)	Parameter	Value(μm)
W	800	W ₈	2
W ₁	37	L	1200
W ₂	70	L ₁	250
W ₃	10	L ₂	100
W ₄	10	L ₃	140
W ₅	60	L ₄	50
W ₆	50	L ₅	60
W ₇	280	L ₆	5

III.RESULT

Figure 3 illustrates the actual chip layout, which is designed using the Taiwan Semiconductor Manufacturing Company 180 nm CMOS process. The measurements were conducted at the Taiwan Semiconductor Research Institute (TSRI) using the Agilent E7350A vector network analyzer (VNA). The experimental setup and test environment are depicted in Fig 4. During the testing, the chip was placed on the signal source

system platform. GSG probes with a spacing of 100 μm were used to make connections, and the chip was connected to the VNA for measurement.

The simulated reflection coefficient is below -10 dB standard for the 99.3 - 114.8 GHz frequency range, and it reaches the lowest resonance point at 108 GHz with a reflection coefficient of -30.6 dB. The measured data shows a bandwidth between 91.1 GHz and 107.1 GHz, with the lowest resonance point at 100 GHz and a reflection coefficient of -22.1 dB. Due to the limitations of the VNA used, which has a measure frequency range from 2 - 110 GHz, it was not possible to measure beyond 110 GHz and therefore it is not shown in the graph. The measured lowest resonance point shows better results compared to the simulation. However, due to fabrication limitations, there is a frequency offset observed in the measured results towards lower frequencies. Nonetheless, the overall trend of the measured results is similar to the simulated values. Therefore, it can be inferred that the measured results beyond 150 GHz would also align with the simulated data. The antenna exhibits a gain of approximately -5 dBi to -4 dBi. At the resonance point of 108 GHz, the gain is -4.6 dBi, as shown in Fig 5.

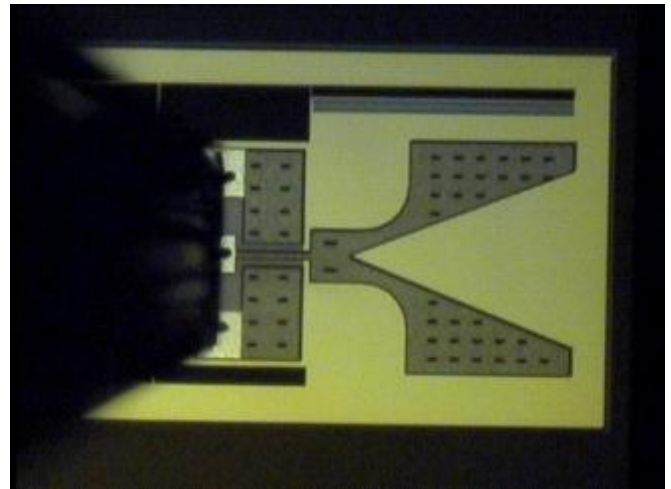


Figure 3. Proposed antenna chip diagram.

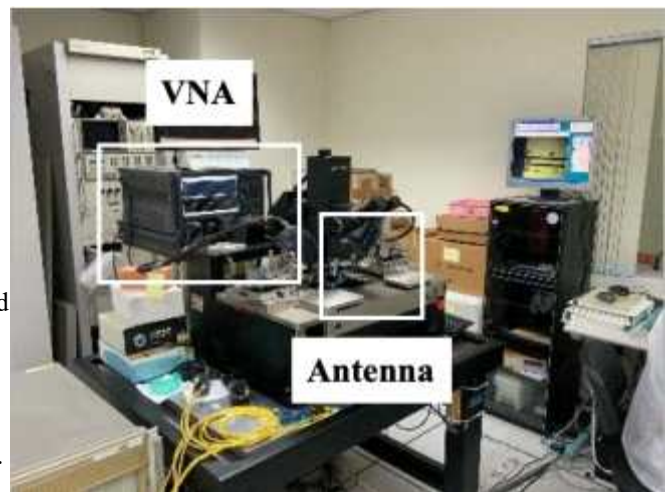


Figure 4. Measurement environment setup

Figure 7(a), 7(b), and 7(c) show that the analysis of surface current distribution for three frequency bands: 99 GHz, 108 GHz (at the lowest resonance point), and 114 GHz. Fig 7(a) illustrates the current distribution at 99 GHz, showing a uniform distribution of surface currents. Fig 7(b) represents the current distribution at 108 GHz, where the currents are primarily excited at the edges of the antenna. Fig 7(c) illustrates the distribution of current at 114 GHz, exhibiting a similar trend to Fig 7(a), with currents approximately evenly distributed across the antenna surface.

High-frequency electromagnetic simulation software was used to simulate the 3D radiation pattern of the antenna at frequencies of 99 GHz, 108 GHz, and 114 GHz, as depicted in Figure 8(a), 8(b), and 8(c) consecutively. In Fig 8(a), the radiation pattern illustrates that the main radiation direction is concentrated on the left side of the chip antenna, with maximum gain of -4.9 dB. In Fig 8(b), the radiation direction shifts towards the top of the antenna, with maximum gain of -4.6 dB. Fig 8(c) exhibits a radiation pattern similar to Fig 8(b), with maximum gain of -4.5 dB.

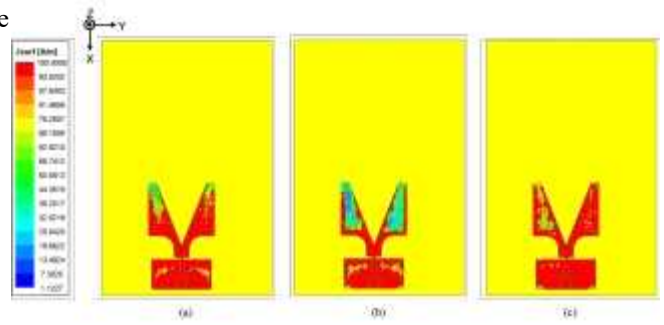


Figure 7. Current distribution (a) 99 GHz (b) 108 GHz and (c) 114 GHz

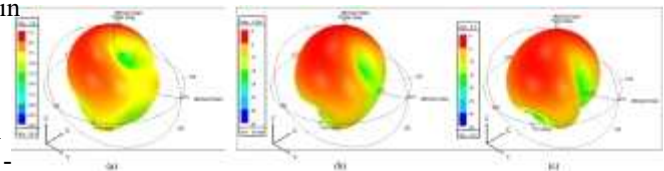


Figure 8. 3D radiation patterns (a) 99 GHz (b) 108 GHz and (c) 114 GHz

IV. CONCLUSIONS

This paper proposes a W-band chip antenna with a Vivaldi-like antenna structure and fabricated in CMOS technology. The size of the chip is $800\ \mu\text{m} \times 1200\ \mu\text{m}$. After simulation and measurement, the simulated data, based on a reflection coefficient standard of -10 dB, covers a frequency range between 99.3 and 114.8 GHz, with a bandwidth percentage of 14.08%. The antenna exhibits a gain of approximately -4.5 dBi in this frequency range. The measured data show a bandwidth ranging from 91.1 - 107.1 GHz, with a bandwidth percentage of 16.14%. In the future, it will be possible to explore the impact of different CMOS processes on chip antennas. By employing different structural designs, it will be feasible to achieve improved performance

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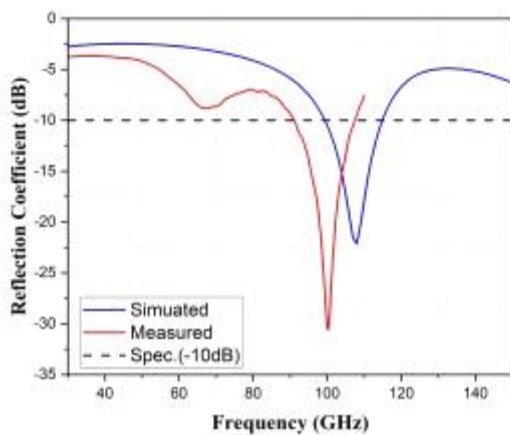


Figure 5. Simulated and measured reflection coefficient data

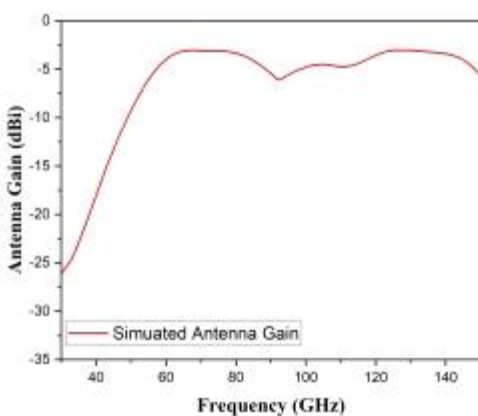


Figure 6. Simulated antenna gain plot

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