

Broadband On-Chip antenna array design in CMOS technology for D-band application

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Abstract— A patch array antenna working in the D-band is proposed in TSMC's 180 nm CMOS. The antenna structure applies a top metal layer (Metal6) as the patch antenna and a bottom metal layer (Metal1) for the ground. Simulation results demonstrate that the on-chip patch antenna has a peak gain of -5.95 dBi at 141 GHz. The measurement of the proposed antenna demonstrates bandwidth from 140 GHz to 202.5 GHz. The array on-chip patch antenna proposed can use in Smart cities technology and automotive applications.

Keywords— D-band, CMOS, Antenna-on-chip, Broadband

I. INTRODUCTION

Higher data transmission requirements have been realized in the 5G mmWave frequency band, such as 28 GHz and 40 GHz. This frequency band has a sub-span size of 800 MHz and a maximum transmission rate of 10 Gbit/s. With the increasing demand for high-speed transmission, greater transmission rates and bandwidth are required to meet the demand. For example, antennas operating in the D-band (110-170 GHz) frequency range greater than 100 GHz can provide highly aggregated bandwidth, enabling transmission rates up to 100 Gbit/s [1, 2].

The wavelength in the D-band frequency band is shorter, so the antenna can be applied to the chip at a relatively low price. The process relationship makes the gain of the chip antenna poor, which may lead to insufficient received signal strength. To avoid the problem of insufficient antenna gain, it is necessary to increase the transmit power to solve the negative impact of the communication system [3, 4].

Recently, there has been lots of research for mmWave chip antenna. The reference [5] utilized a patch antenna array and a planar monopole antenna. The planar monopole antenna incorporated multiple membrane supports and a polymer cavity. Under the patch array antenna configuration, at 130 GHz has an 8.66 dBi maximum gain and 126.5 to 138 GHz bandwidth. To raise the radiation effect of the slot antenna, a cavity is introduced, which can improve the gain to a maximum value of -2 dBi [6]. In the 130 GHz meandering slot antenna, a stacked dielectric resonator (DR) can improve the antenna's high efficiency and gain. Experimental results show that 130 GHz has a 43% radiation efficiency and a 4.7 dBi

gain [7]. The dual-frequency helical monopole chip antenna utilizes the hybrid structure of the helix and the package substrate, and the linear monopole antenna can raise the antenna radiation's high efficiency and obtain a dual-frequency band. The antenna gets an efficiency of 45% at 28 GHz and 30% at 60 GHz [8]. A square ring resonator (SRR) can also be used to address the gain drop problem. Experimental results show that a gain reduction of about 7 dBi can be compensated at 85 GHz; at 81.5 GHz, a maximum gain of 1.61 dBi can be compensated [9]. The experimental results indicate that approximately 7 dBi of gain reduction can be compensated for at 85 GHz, while 1.61 dBi, a maximum gain, can be compensated for at 81.5 GHz.

This paper proposes a broadband on-chip array antenna in the D-band frequency. The antenna is implemented using CMOS technology. The simulation results demonstrate that at 141 GHz, the antenna can obtain a peak gain at -5.95 dBi. The bandwidth measured below the -10 dB standard ranges from 140 to 202.5 GHz. It can be applied in Industrial, healthcare, and automotive application [10].

II. ANTENNA DESIGN

This paper introduces the CMOS broadband on-chip antenna in D-band implemented. Figure 1 shows the structure of the on-chip patch array antenna using the top metal layer (Metal6) with a thickness of 2.34 μm as the antenna and the bottom metal layer (Metal1) with a thickness of 0.53 μm as the ground. The size of the patch array antenna is $1200 \times 1200 \mu\text{m}^2$. Figure 2 and Table 1, illustrate the antenna geometry. Preliminary simulation results indicate that the chip antenna exhibits two frequencies resonant at 141 GHz and 180 GHz. In Figure 3, The lowest points of the reflection coefficient are -34.3 dB and -15 dB, respectively. The gain, depicted in Figure 4, reaches its peak at 137 GHz with a value of -5.41 dBi.

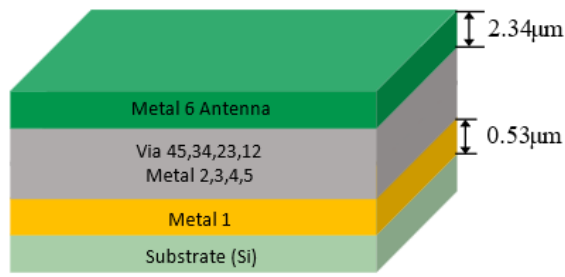


Figure 1. Process stack diagram

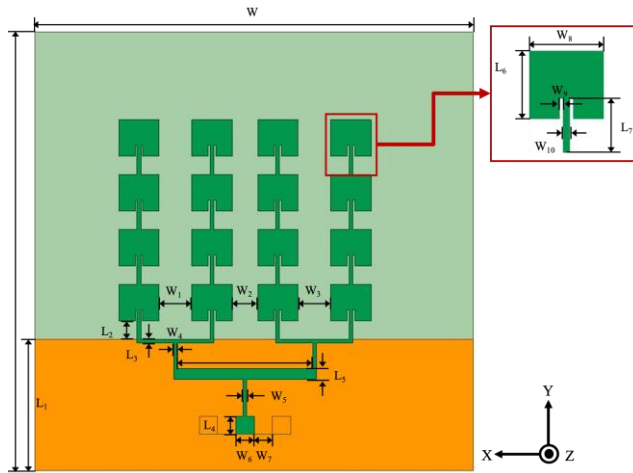


Figure 2. Antenna geometry

TABLE 1. SUMMARY OF GEOMETRIC DIMENSIONS

Unit: μm			
Parameter	Value	Parameter	Value
W	1200	L	1200
W1	90	L1	360
W2	70	L2	60
W3	90	L3	10
W4	10	L4	50
W5	10	L5	30
W6	50	L6	100
W7	50	L7	80
W8	110		
W9	5		
W10	10		

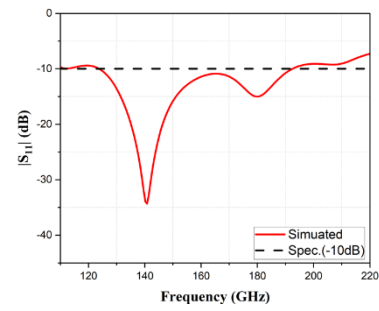


Figure 3. Reflection coefficient (S11)

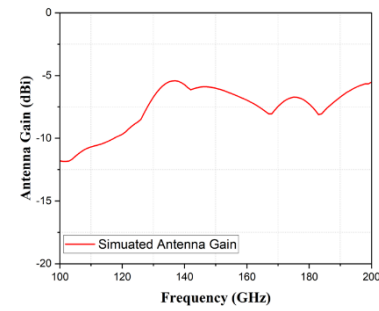


Figure 4. Gain plot

III. SIMULATION AND MEASUREMENT RESULTS

The prototype of a broadband on-chip antenna fabricated by the CMOS technology. The proposed antenna was designed for D-band operation. To prevent metal layers from interfering with each other and reduce losses, the antenna structure uses a top metal layer (Metal6) and a bottom metal layer (Metal1). The size of the chip antenna is $1200 \times 1200 \mu\text{m}^2$. Figure 5 shows a micrograph of the chip antenna.

The measurement environment adopts the following equipment settings: Keysight PNA-X N5242B (10 MHz~26.5 GHz) vector network analyzer, and G-band frequency extension module (140 GHz~220 GHz), as shown in Figure 6.

During measurement, the chip is placed on the signal source system platform with absorbing material and fed using GSG probes. In Figure 7, According to the simulation, that can be observed that the chip antenna exhibits two frequencies resonant at 141 GHz and 180 GHz. The bandwidth simulated is 43.2%, with a range of 124 GHz to 192.4 GHz. The measured bandwidth is 36.5%, ranging from 140 to 202.5 GHz. Since the instrument can only measure 140 - 220GHz, measurement results below 140GHz cannot be obtained. Based on the trend of measurement results from 140 - 220GHz, it is speculated that the results below 140GHz should be similar to the simulation results.

Figure 8 and Figure 9 show the 2D antenna radiation pattern planes of xz and yz at 141 GHz. The antenna can be observed that the peak gain in the xz plane is -6.14 dBi. The peak gain is -5.95 dBi in the yz plane.

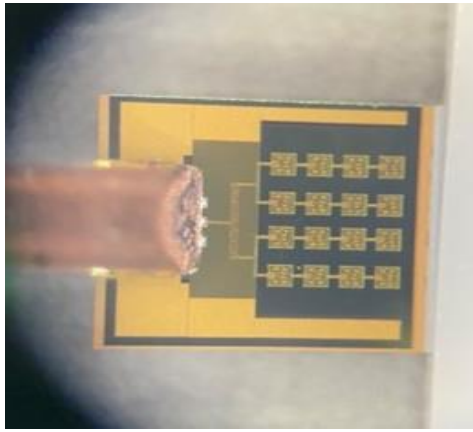


Figure 5. Chip photograph

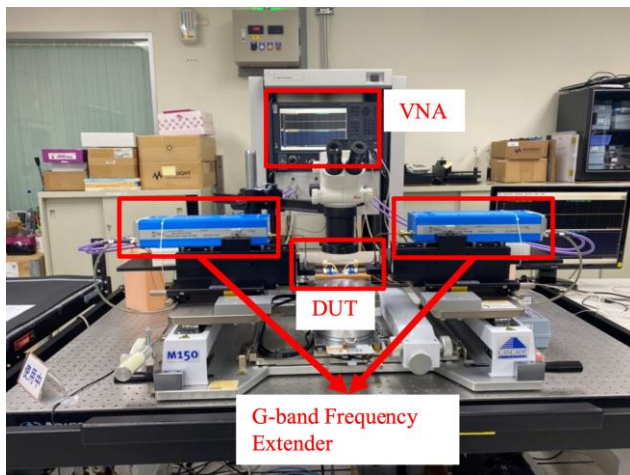


Figure 6. Measurement equipment diagram

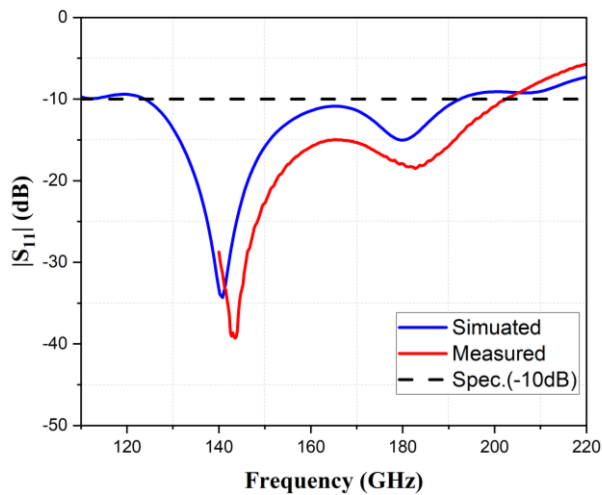


Figure 7. Simulation and measurement overlay plot

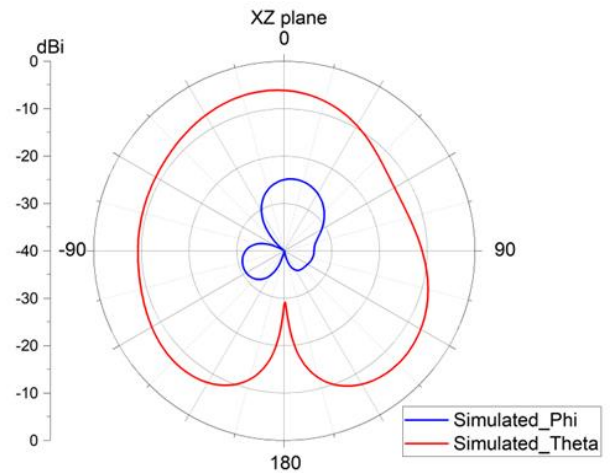


Figure 8. XZ plane

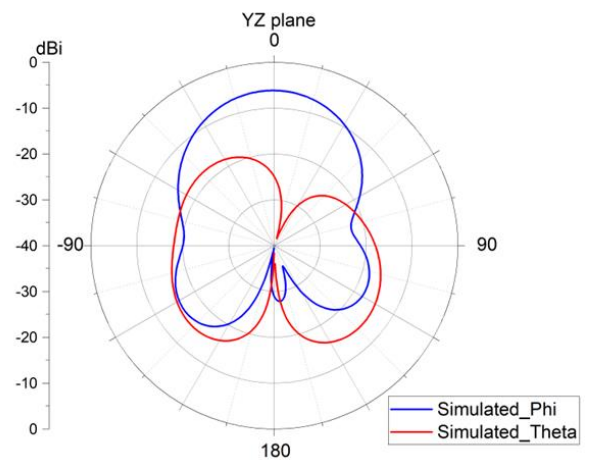


Figure 9. YZ plane

IV. CONCLUSIONS

This study proposed a broadband on-chip antenna array that functions within the D-band. The antenna is implemented by the 180 nm CMOS process of TSMC. The simulation result shows that 141 GHz has a -5.95 dBi maximum gain, with a bandwidth percentage of 43.2% ranging from 124 GHz to 192.4 GHz. The measured bandwidth is 36.5%, range of bandwidth from 140 GHz to 202.5 GHz. The proposed antenna can be applied in Smart cities, smart homes, electronic healthcare, intelligent transportation, and smart factory[11-13].

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