

Design of Ka-band Chip Antenna Based on Slot Antenna

Ming-An Chung*

Department of Electronic Engineering
National Taipei University of
Technology
Taipei, Taiwan
mingannchung@ntut.edu.tw

Kai-Xiang Chen

Department of Electronic Engineering
National Taipei University of
Technology
Taipei, Taiwan
t112368524@ntut.edu.tw

Kuo-Chun Tseng

Department of Electronic Engineering
National Taipei University of
Technology
Taipei, Taiwan
t110368157@ntut.edu.tw

Abstract— A broadband chip antenna designed for millimeter wave (mmW) can be used in fifth-generation (5G) frequency bands. The on-chip mmW antenna designed for the Ka-band utilizes standard Complementary Metal-Oxide-Semiconductor (CMOS) technology. In this design, the mmW antenna structure is formed by connecting the top layer (Metal6) and the bottom metal layer (Metal1) to reduce losses. Many architectures have been proposed for chip antennas to overcome the metal thickness during fabrication and improve the gain of chip antennas. Therefore, this paper proposes an on-chip antenna for the fifth-generation mobile communication millimeter-wave frequency band. Using high-frequency electromagnetic simulation software, the chip antenna exhibits a minimum return loss of -18dB at 31GHz and a peak gain of -7 dBi. The measured reflection coefficient is below -10dB from 18.8 GHz to 32.5 GHz.

Keywords— Antenna on-chip, millimeter-wave, CMOS

I. INTRODUCTION

The 5G communication millimeter wave frequency band has recently attracted the attention of academia and the industry and has also become the focus of discussion in the field of the Internet of Things and future communication frequency band technology. It not only provides faster data connections but also enables services with virtually no latency characteristics [1, 2].

Antennas play a vital role in communication systems and can be used to send and receive signals, improving communication quality by compensating for propagation losses [3]. Due to the higher frequency range used in mmW or future terahertz (THz) applications, the antennas used are very small in size [4]. Furthermore, with the development of high system integration, mmW antenna, and feed circuit technologies have become increasingly mature, making chip antennas a favorable choice.

In [5], the study investigates how chip antennas achieve high gain and wideband performance. The application of a pair of switches is used to design frequency reconfigurability on the antenna, enhancing the antenna's bandwidth. The chip utilizes CMOS technology with high resistivity (HR) to improve antenna gain. A chip-integrated spherical dielectric resonator is used, and the antenna is excited by an on-chip annular resonator. Two vertical microstrip line feeds generate radiation, increasing the antenna's bandwidth [6].

This paper designs a broadband on-chip array antenna for Ka-band. The antenna is implemented using CMOS technology. It exhibits a minimum reflection coefficient of -18 dB at 31 GHz and -7 dBi peak gain. The measured reflection coefficient is under -10dB, and the frequency range is 18.8 GHz to 32.5 GHz, making it highly suitable for applications in the 5G mobile communication mmW frequency band.

II. ANTENNA DESIGN

This paper presents an on-chip wideband antenna designed using CMOS technology for the 38 GHz millimeter-wave frequency band. The overall on-chip antenna comprises Metal6 with a thickness of 2.34 μm for the design of the antenna body and a bottom layer (Metal1) with a thickness of 0.53 μm for grounding, as shown in Figure 1.

Figure 2 and Table 1 depict the geometric structure and parameters of the antenna. The chip antenna occupies an area of $1150 \times 1000 \mu\text{m}^2$. Simulation results show that the return loss of the design is 18.8-32.5 GHz in the frequency range below -10 dB. In Figure 5, the lowest point of the reflection coefficient is -27dB at 26 GHz. The gain is illustrated in Figure 6, reaching a peak value of -7 dBi at approximately 40 GHz.

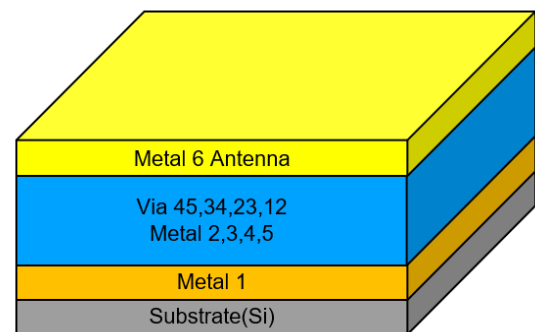


Figure 1. Layer structure of 0.18- μm CMOS.

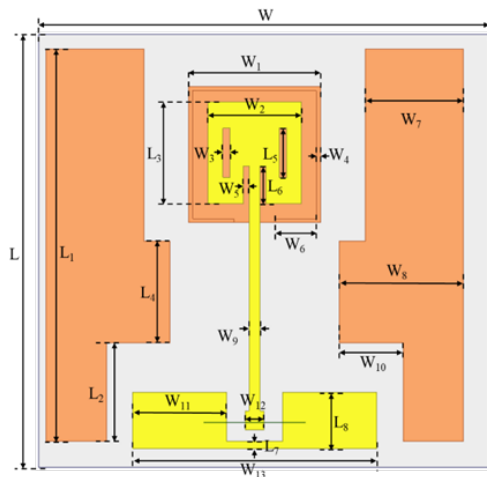


Figure 2. Slot antenna CMOS architecture.

TABLE 1. ON-CHIP ANTENNA PARAMETERS.

Parameter	Value(μm)	Parameter	Value(μm)
W	1200	L	1150
W ₁	350	L ₁	1040
W ₂	250	L ₂	260
W ₃	20	L ₃	270
W ₄	10	L ₄	270
W ₅	15	L ₅	130
W ₆	110	L ₆	100
W ₇	260	L ₇	20
W ₈	330	L ₈	150
W ₉	30		
W ₁₀	170		
W ₁₁	250		
W ₁₂	50		
W ₁₃	650		

III.RESULT

This article describes an antenna design on-chip. The proposed antenna is intended for the mmW frequency band of fifth-generation mobile communication. Figure 3 shows a microscopic image of the chip. During measurement, the on-chip antenna is placed on the signal source platform using a suction pen, and the GSG RF probe feeds the chip antenna while being externally connected to a network analyzer for measurement. Prior to measurement, LRRM calibration is performed, followed by verification using microstrip lines (Thru, Open, Short). The chip measurement is conducted after

confirming that all verifications are within the acceptable range of errors. The equipment used for chip antenna measurement is the Network Analyzer (Keysight N5247A), which has a measurement bandwidth of 10MHz to 67GHz. The software used for chip antenna measurement is Cascade WinCal XE and Agilent IC-CAP. Figure 4 illustrates the measurement environment setup.

Observing the actual measured S11 values, as shown in Figure 5, the simulation trend slightly deviates towards lower frequencies. The simulated antenna is a 38GHz slot chip antenna. The measured reflection coefficient meets the standard below -10dB, and the bandwidth is 18.8-32.5GHz. The area of the chip antenna is 1150×1000 μm . In the simulation, the M1 layer is used as the ground to realize the reflection band, and the slot effect is used to enhance the antenna gain so that the patch antenna can obtain the maximum gain. The simulated gain of the patch CMOS on-chip antenna is about -7dBi, as shown in Figure 6. The gain of an mmW patch antenna cannot be measured directly due to the current limitations of the instrumentation, so the gain graphs are based on simulated values.

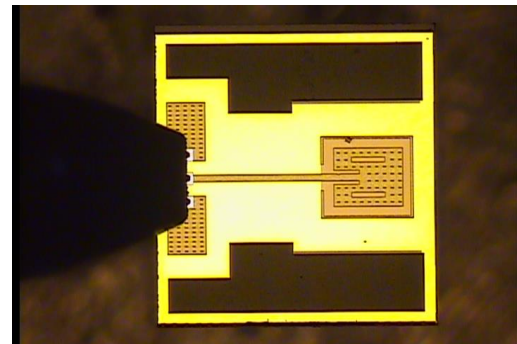


Figure 3. Micrograph of the proposed chip antenna.



Figure 4. Measurement environment architecture.

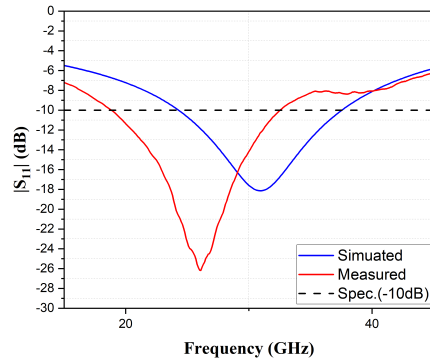


Figure 5. Hi

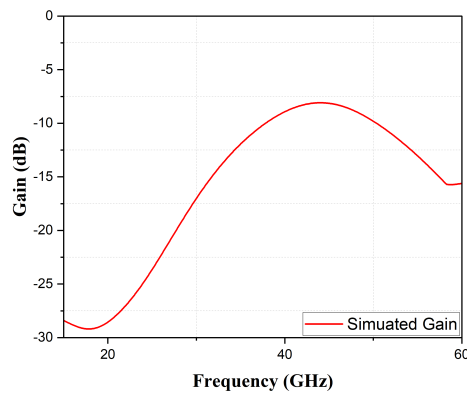


Figure 6.

Figure 7 shows the current distribution on the surface of the CMOS antenna. As can be seen, the current is largely stimulated at the antenna's feeding location when the frequency is at 26GHz, and coupling takes place between the antenna and its surroundings as well as between the Metal 1 ground plane and the antenna's central slot to produce bandwidth. The antenna's overall current distribution is uniform.

The 2D radiation patterns of this on-chip antenna are shown in Figure 8. The figure displays the antenna xz-plane and yz-plane of the antenna at 26GHz. The 3D radiation pattern in Figure 9 shows that at 26GHz, the overall radiation is uniformly distributed directly above the chip antenna, and the radiation energy is highly concentrated without any radiation divergence.

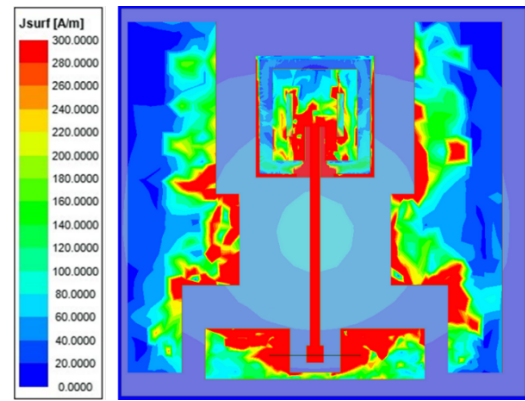


Figure 7. Current distribution (a) 99 GHz (b) 108 GHz and (c) 114 GHz

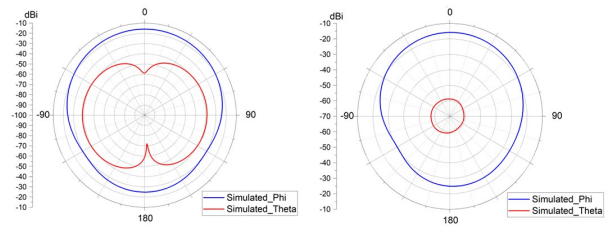


Figure 8. 3D radiation patterns (a) 99 GHz (b) 108 GHz and (c) 114 GHz

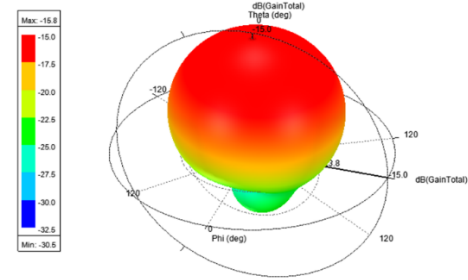


Figure 9.

IV. CONCLUSIONS

This research suggests a Ka-band chip antenna with a slot antenna-like structure that can be produced using the TSMC 0.18-μm CMOS technology process. The CMOS on-chip antenna measures 1150 by 1000 μm. Through the simulations and measurements, the antenna's simulated frequency range of 25-38 GHz with a bandwidth percentage of 52% and an antenna gain of approximately -6 dBi, satisfying the reflection coefficient standard below -10 dB. The measured data demonstrates a bandwidth range of 18.8-32.5 GHz with a bandwidth percentage of 54.8%. In order to raise the antenna bandwidth and gain performance and realize diversified applications, it will be possible to study the development and impact of various CMOS processes on-chip antennas in the future.

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MING-AN CHUNG (Member, IEEE) received the B.Eng. and M.Eng. degrees in electronic engineering from the Chang Gung University, Taoyuan, Taiwan and the D.Eng. degree in electrical engineering from the National Taiwan University of Science and Technology (NTUST), Taipei, Taiwan, in 2003, 2005, and 2016, respectively. He is currently an Associate Professor with the Department of Electronic Engineering, National Taipei University of Technology (NTUT), where he also serves as the Leader of the Innovation Wireless Communication and

Electromagnetic Applications Laboratory. His research interests include wireless communication propagation, intelligent robotics, self-driving vehicles, antenna design for various mobile and wireless communications, electromagnetic theory, and applications. He is also a Reviewer of many scientific journals, including the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION, IEEE Transactions on Industrial Informatics, Journal of Intelligent & Robotic Systems, IET Microwaves, Antennas and Propagation, IEEE Antennas and Wireless Propagation Letters, International Review of Electrical Engineering, International Journal on Communications Antenna and Propagation and AEÜ - International Journal of Electronics and Communications, and many international conferences, including ICRA, ICCE-TW, RFIT, ICBEB, EMCAR and SNSP.



KAI-XIANG CHEN received the B.Eng. from National Taipei University of Technology (NTUT), Taipei, Taiwan, in 2023. Prior to this, he worked at Inventec as a firmware engineer, where he contributed to the development of OpenBMC, gaining substantial experience in both hardware and software domains. Currently, he is pursuing a Master's degree at National Taipei University of

Technology, specializing in the field of electromagnetics. His research interests encompass antenna technology, artificial intelligence (AI), unmanned devices, and the Internet of Things (IoT).



KUO-CHUN TSENG received the B.S. degree in Computer and Communication from the National Pingtung University, Pingtung, Taiwan, in 2021. He is pursuing an M.S. degree in electronic engineering with the National Taipei University of Technology, Taiwan. His current research interest includes the design of CMOS RF/microwave integrated circuits and antenna phased arrays for the applications of the fifth generation of mobile communications.