

An Analysis of DDR Channel Signal Integrity on a High-Performance Computing Mainboard

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Abstract— This paper focuses on the design of a mainboard of a computing node, a component of the server platform that can compute high-performance big data operations at high speed. In particular, it describes the results of a signal integrity analysis of the signal channels between the memory and the CPU on the PCB of the mainboard equipped with multiple DDR5 memories to rapidly process complex operations. Signal integrity verification is possible by checking whether the signal including high frequency is reflected on the PCB line, data loss, or affected by the signals of adjacent channels when transmitted. This paper discusses the preparation elements, analysis method, and analysis results required for DDR channel signal integrity analysis.

Keywords— signal integrity, insertion loss, DDR, eye diagram, computing node

I. INTRODUCTION

As artificial intelligence technology evolves, various learning methods are being developed on the software side to increase the learning speed and accuracy of artificial intelligence algorithms for massive data. In addition, as hardware technology is also rapidly developing, hardware platforms are using computing nodes consisting of CPUs and GPUs.

Cloud computing requires the production of higher-performance servers, and data acceleration technology is needed to implement high performance. Consequently research is being conducted to propose a system that reduces the CPU usage of the host server and efficiently manages the server's resources. This can enable efficient packet transmission [1].

There are many factors to consider when designing and manufacturing the mainboard hardware of a computing node. When using multilayer PCBs, low dielectric constant PCB materials must be selected to minimize signal loss, and power and signal layers must be separated. Furthermore, PCB stack-up, PCB layout considering proper placement of numerous components, signal integrity, and power integrity must be considered.

Among the verification items for the mainboard PCB, signal integrity and power integrity should be especially considered when designing the PCB layout for transmitting high-speed signals since interference occurs frequently as high-speed signal lines are designed adjacent to each other. In

addition, errors can be reduced during hardware design and production, and production time can be shortened by predicting characteristics in advance. Thus, analysing the signal integrity of DDR channels with fast transmission bandwidth is necessary, and can be confirmed through S-parameters and eye diagrams for each signal channel during analysis.

This paper describes the configuration and features of the mainboard of the computing node, a component of the Supreme-K system under research and development in the <Supercomputer Development Pilot Project>. In order to increase the computing speed, the mainboard is designed to be equipped with an accelerator chip manufactured with domestic technology.

II. PREPARATIONS FOR SIGNAL INTEGRITY ANALYSIS

A. Configuration of the Computing Node and Features of the Computing Node Mainboard

A conceptual diagram of a single cluster rack, a component of the supercomputer, is shown in Figure 1 below. A single cluster contains computing nodes, management nodes, storage nodes, and login nodes [2].



Figure 1. Configuration of a single cluster in a supercomputer.

Since high-speed signals of 7 GHz or faster are transmitted along the PCB lines where the memory is connected, signal strength loss occurs due to signal reflection and coupling. In addition, since the 0.1 mm thick lines are closely spaced at 0.2 mm intervals, they can interfere with each other and cause crosstalk. Therefore, it is necessary to analyze the characteristics of the high-speed signal lines on the PCB drawing in advance before printing the PCB.

Regarding DDR4 and DDR5 memories, the loss in signal strength can be reduced by selecting the value of ODT (on-die termination) of DRAM [3]. For DRAM mounted on the PCB, DIMM performance can have a great impact. In this case, power integrity as well as signal integrity should be considered in the design [4]. Also, DDR channels are vulnerable to ISI (intersymbol interference) effects. Therefore, equalization techniques that mitigate reflections are useful for high data transmission speeds [5].

In order to perform a signal integrity analysis, PCB files (ODB++ or BRD), schematics, IBIS models for IC chips, package loss, models for cables or connectors, PCB stack-up information, etc., must be prepared in advance. In addition, a simulation program that can analyze signal integrity by utilizing this information is required.

B. Preparing DDR Channel Signal Integrity Analysis

For compute nodes, the motherboard hardware provides DDR5 memory slots that support high speed at low power to optimize computational performance. Since six channels of DDR memory are connected for each accelerator chip, a motherboard equipped with two accelerator chips supports a total of 12 DDR5 DIMM memory slots [6].

The number of target lines for DDR-related signal integrity analysis is 171 per channel, with 12 DIMM channels, for a total of 2,052 nets to be analyzed. Each line includes multiple CK, CS, CA, DQ, and DQS signals. The insertion loss, crosstalk, and eye diagram for the PCB trace of each signal line must be examined. Additionally, the line length for all nets must be designed to be less than 4.5 inches. For the PCB, EM890K (ER = 2.9) material was used to reduce high-speed signal loss, and a 16-layer multi-layer board (2.2 mm thick) was designed to minimize signal interference between the power layer and the signal layer. The mainboard was mounted inside the chassis, and the chassis size was 482 mm x 790 mm x 133 mm [7].

C. Selecting Nets for Simulation and Creating S-parameter Models

To perform a signal integrity simulation, Siemens EDA's simulation program HyperLynx ver.2.14 was used. In Figure 2 below, there are six DDR memories connected to one accelerator chip DDR controller. Among these, the length of DQ net has a value between 45 mm and 49 mm.

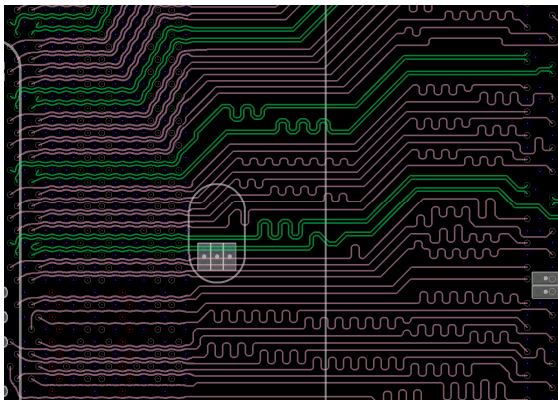


Figure 2. Partial nets between CPU and DDR5 CH0 placed in Layer 14.

If four nets are selected from dozens of nets and converted into a two-dimensional free form schematic, the result is as shown in Figure 3. If this schematic is extracted as an S-parameter model, an s8p model is created as it comprises eight ports.

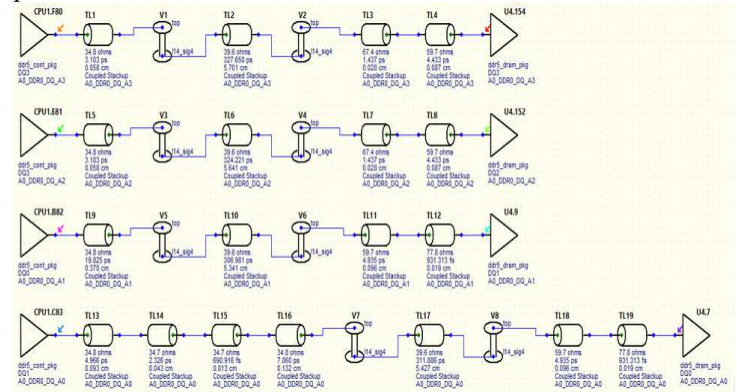


Figure 3. Free form schematic conversion diagram of PCB net.

In a real environment, since the chip's package loss component must be reflected, the PCB channel model and package model generated above must be connected for simulation. The configuration is as shown in Figure 4. This is a simulation configuration diagram combining the package model (s342p) and the DDR channel model (s8p).

The Siemens EDA HyperLynx DDR5 model was used as the input/output IBIS buffer model. The models used were IBIS-AMI models ddr5_generic_ctrl.ibs and ddr5_generic_dram.ibs.

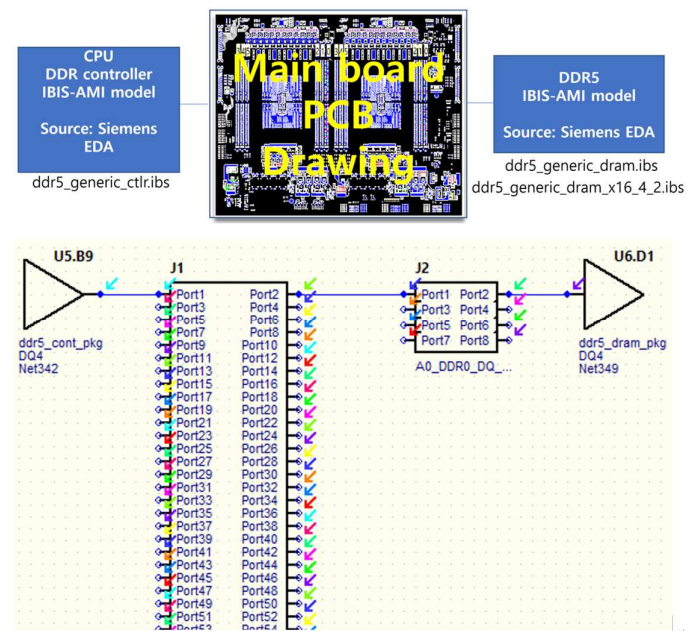


Figure 4. Simulation configuration combining package loss model and PCB DDR channel loss model.

III. SIGNAL INTEGRITY SIMULATION RESULTS

The signal integrity simulation items of DDR channels are insertion loss, input reflection coefficients, crosstalk, and eye

diagrams. Insertion loss represents the ratio of the output value that is lost after the signal intensity passes through the trace of the PCB. The input reflection coefficient is the relative ratio of the signal that enters the trace and is reflected again. Crosstalk represents the degree to which the value affected by the adjacent traces is reflected. An eye diagram is a representation of voltage waveforms superimposed on a time axis to evaluate the quality of a digital signal. In the signal analysis of DDR5, the input/output buffer model can confirm the eye diagram for the DDR5 channel using the IBIS-AMI model.

A. Insertion Loss and Input Reflection Coefficients

For the PCB pattern of the DDR5 DQ signal, the line width was 0.1 mm and the spacing between the lines was 0.2 mm. The characteristic impedance was designed to be approximately 40 ohm. To confirm the trace characteristics for the DDR5 channel on the PCB, the S-parameter simulation results for the 2-port DDR net were confirmed. The data transmission speed of DDR5 ranges from 3200 MTPS to 7200 MTPS. When confirming this in terms of frequency, the insertion loss and input reflection coefficient measured above 7.2 GHz. As shown in Figure 5, the insertion loss value was -2.7 dB and the input reflection coefficient (S11) was -5.8 dB at 8 GHz.

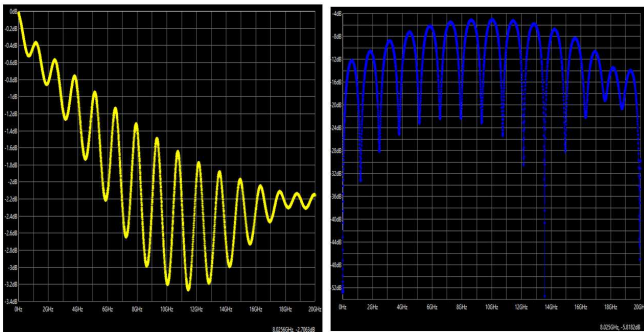


Figure 5. Simulation results for insertion loss and input reflection coefficient

B. Crosstalk (NEXT or FEXT)

Crosstalk is an expression of the degree to which adjacent lines affect the main line. Regarding crosstalk verification results, NEXT (near-end crosstalk) was -40.3 dB at 7.95 GHz, and the FEXT (far-end crosstalk) simulation result was -44.7 dB at 8 GHz, as shown in Figure 6 below.

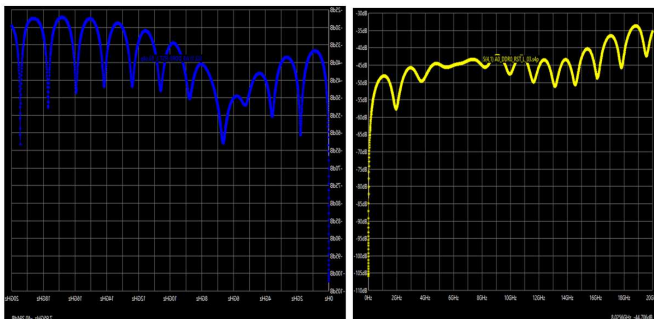


Figure 6. Simulation results for insertion loss and input reflection coefficient

C. Eye Diagram Analysis Results According to Schematic Composition Changes

Figure 7 shows various schematic configuration changes. (a) shows only the input/output buffer model, and there is no physical device connection between the buffers. (b) is the case showing the PCB loss information reflected between the input/output buffers. (c) shows the SOC chip package loss of the DDR controller was added between the input/output buffers. (d) shows that the input/output buffers were terminated without opening the unused ports.

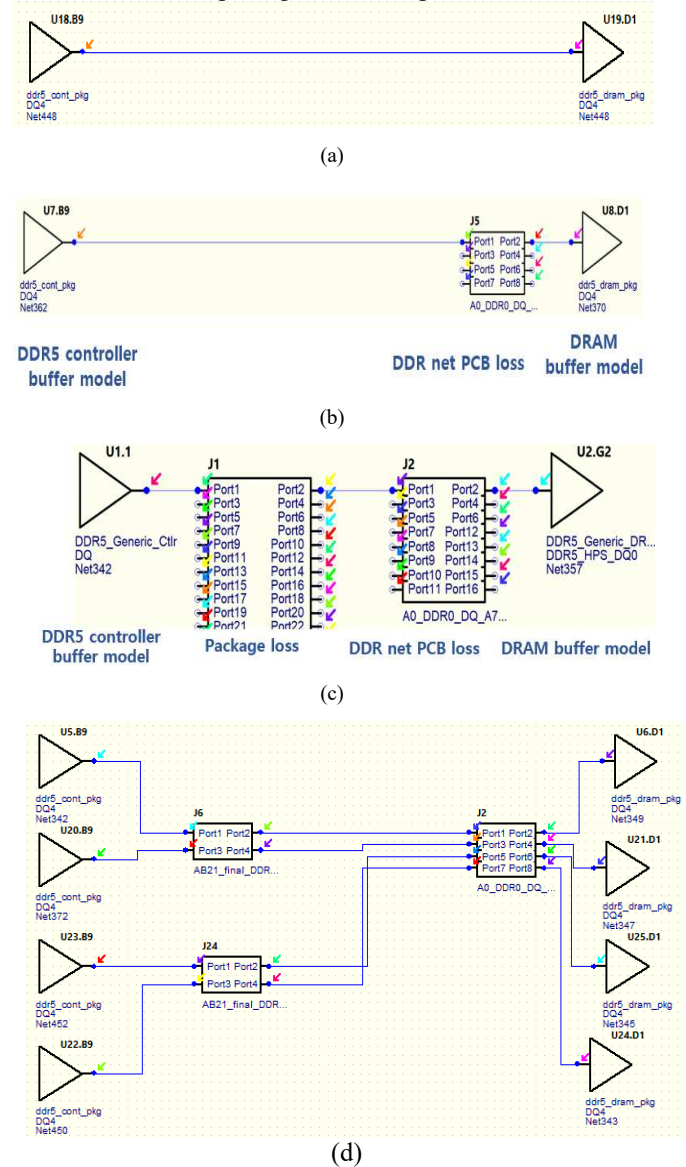


Figure 7. Cases for configuring simulations according to various schematic configurations.

The eye diagram simulation revealed that the 1 UI (unit interval) of DDR5-3200 had a value of 313 ps, and the voltage corresponding to the eye height ranged from 0 V to 1.1 V, as can be seen in Figure 8. In the case of (a) with only the input/output buffer model, the eye width and eye height were 288.5 ps and 696.8 mV, respectively. In (b), the eye width and

eye height were 277.9 ps and 716.3 mV, respectively. In the case of (c), the eye width and eye height were 269.7 ps and 643.0 mV, respectively. In the case of (d), the eye width and eye height are 244.9 ps and 393.7 mV, respectively. The eye height and eye width values for each case were as shown in Table 1.

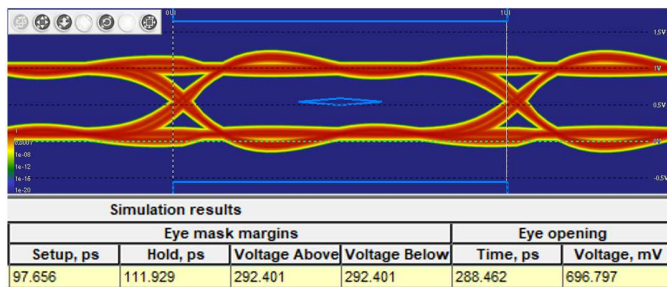


Figure 8. Eye diagram characteristics; eye mask margin and eye opening.

TABLE 1. EYE HEIGHT AND EYE WIDTH

Case	Simulation Results (Eye Diagram / Eye Opening)		
	Descriptions	Time [ps]	Voltage [mV]
(a)	Channel model: None Single buffer model	288.5	696.8
(b)	Channel model: PCB loss model Single buffer model	277.9	716.3
(c)	Channel model: PCB models + Chip package model Single buffer model	269.7	643.0
(d)	Channel model: PCB models + Chip package model Multi-buffer models	244.9	393.7

IV. CONCLUSIONS

This paper described the signal integrity analysis for the PCB layout designed for the main board of a high-performance computing node. In particular, it focuses on the signal integrity analysis results for the channels where DDR5 memory is connected in the PCB layout. In addition, the

preparation elements, analysis methods, and analysis results required for signal integrity analysis were described in detail. These can be used to design and verify the PCB.

The signal integrity analysis confirmed the insertion loss, input reflection coefficient, NEXT, and FEXT values. In order to confirm changes in the eye diagram according to various conditions, a comparison was made between when the channel loss was not reflected and when it was reflected. In the future, more accurate results will be possible by applying the connector model, cable model, and IBIS model of the actual memory used. In addition, in the case of a PCB with a high-speed transmission signal, the influence of the back drilling and via pad on the back of the PCB should be considered. In this case, if the size of the PCB is considerably large, the analysis time may be prolonged if a 3D analysis tool is utilized. In conclusion, signal integrity analysis can be used as a pre-verification tool to shorten the design time and prevent design errors in advance when designing the PCB layout.

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