

A 64 Gbaud PAM4 Fully-Differential Optical Receiver Integrated With Monolithic Dual Photodiode

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Abstract— We present a 64-Gbaud PAM4 monolithic optical receiver using a fully-differential dual-photodiode architecture that eliminates single-to-differential conversion, achieving 34.8-GHz bandwidth, -3.6 -dBm sensitivity, and 0.66 pJ/bit.

Keywords— CMOS, PAM4, optical receiver, integration, Photodiode

I. INTRODUCTION

As artificial intelligence (AI) workloads continue to surge in cloud and hyperscale datacenters, there is a rapidly growing demand for optical interconnects that can support data rates exceeding 100 Gbps per lane while maintaining low power consumption. To address this requirement, four-level pulse-amplitude modulation (PAM4) has become widely adopted, as it enables a twofold increase in transmission capacity without expanding the fundamental channel bandwidth. However, compared to conventional NRZ signaling, PAM4 imposes significantly stricter requirements on receiver linearity and noise performance. The optical receiver is a critical component of such interconnect systems, as it plays a central role in meeting these demanding performance requirements.

Conventional optical receivers typically employ a single photodiode (PD) that produces a photocurrent. As a result, a single-to-differential (S2D) buffer and a low-pass filter for an AC-coupling network are required to interface with differential transimpedance or gain stages. This pseudo-differential architecture inherently introduces bandwidth degradation, additional area and power overhead.

In this work, a monolithically integrated fully-differential silicon photonics optical receiver front-end in a 45-nm CMOS SOI process is presented. The receiver directly generates balanced differential photocurrents using a 1:2 multimode interferometer (MMI), grating coupler (GC), and dual photodiodes (PDs), thereby eliminating the need for any S2D conversion or low-pass filter. A fully-differential transimpedance amplifier (TIA) is employed as the first electronic gain stage, followed by a continuous-time linear equalizer (CTLE) and a variable-gain amplifier (VGA) optimized for PAM4 linearity. The architecture allows current-mode differential signaling to be preserved from the

optical domain through to the electrical output, maximizing bandwidth, linearity, and common-mode noise immunity.

II. PROPOSED RECEIVER ARCHITECTURES

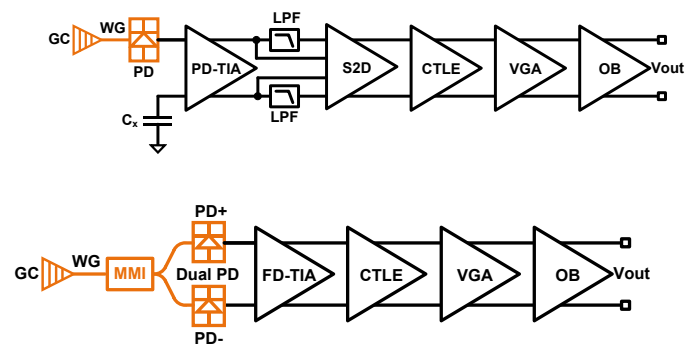


Figure 1. Conceptual comparison of receiver architectures: (a) conventional pseudo-differential architecture and (b) proposed fully-differential architecture.

Fig. 1 conceptually compares a conventional pseudo-differential optical receiver architecture with the proposed fully-differential monolithic implementation. In a conventional receiver, a single photodiode (PD) is used to convert the incoming optical signal into a single-ended photocurrent. This photocurrent is first amplified by a pseudo differential transimpedance amplifier (PD-TIA), whose output must subsequently pass through an AC-coupling or low-pass filter to remove DC-offset error caused by photodiode DC current. A single-to-differential (S2D) buffer is then required to generate a differential signal for next amplifiers. While this approach has been widely adopted for NRZ systems, its mandatory filtering, limited bandwidth, and strongly nonlinear gain behavior make it suboptimal for wideband multi-level PAM4 operation.

In the proposed receiver, a 1:2 multimode interferometer (MMI) evenly splits the optical input onto two matched photodiodes (PD+ and PD-), generating true differential photocurrents with opposite polarities at the source. These differential currents directly drive the inputs of a fully-differential TIA (FD-TIA), eliminating the need for low-pass

filter, DC-offset cancellation, and S2D conversion. The TIA output is then followed by a continuous-time linear equalizer (CTLE) that compensates for high-frequency channel loss, and a variable-gain amplifier (VGA) providing linear gain control while preserving PAM4 amplitude spacing. A $50\ \Omega$ differential output buffer completes the interface toward high-speed test equipment or next digital signal processing (DSP) unit. This monolithically integrated, fully-differential architecture achieves inherently high CMRR, removes the analog filtering overhead, and enables fully linear PAM4 magnitude processing throughout the entire signal chain.

III. MONOLITHIC OPTICAL RECEIVER DESIGN WITH DUAL PHOTODIODE

The proposed receiver is fabricated in a 45-nm CMOS SOI process that supports monolithic integration of electronic and photonic components on a single substrate. The 1:2 MMI splitter, dual photodiodes, O-band waveguides, and fully-differential receiver front-end circuits are co-integrated without requiring any external optical coupling interfaces or interposer-level connections. This co-fabrication approach minimizes parasitic capacitance, routing imbalance, and optical insertion loss, thereby enabling broadband and highly symmetric differential signaling from the point of photo-detection.

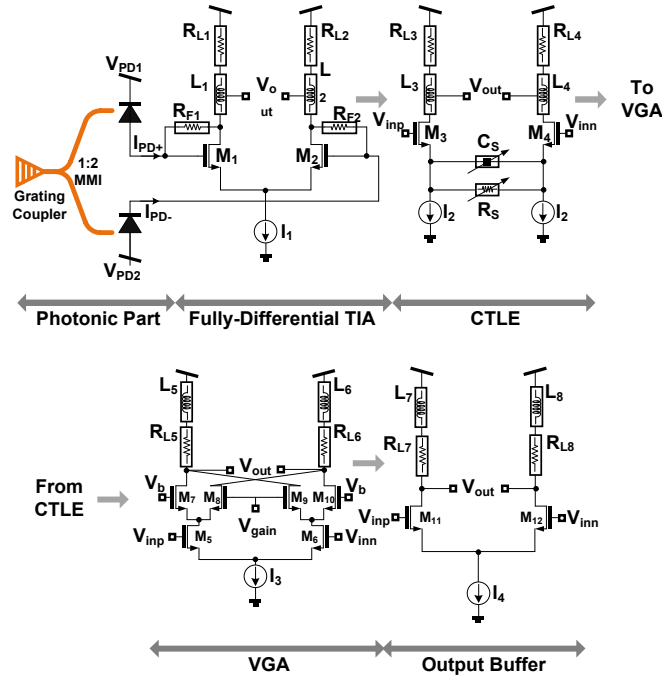


Figure 2. Schematic diagram of the proposed receiver.

The TIA employs a common-source input stage with symmetric series inductors to maximize transimpedance gain while reducing input impedance and thermal noise. A feedback resistor is utilized to achieve a target transimpedance gain of $53\ \text{dB}\Omega$ while maintaining stability across the full input dynamic range. The fully-differential nature of the input

directly supports current-mode rejection of common-mode noise sources, enabling a measured input-referred noise density of $11.5\ \text{pA}/\sqrt{\text{Hz}}$. A continuous-time linear equalizer (CTLE) is placed immediately after the TIA to compensate for dominant pole, photodiode junction capacitance, and on-chip interconnect parasitics. The CTLE employs a tunable zero-pole pair implemented using an adjustable R-C peaking network, enabling up to 6 dB of controllable gain peaking near the Nyquist frequency. This approach enhances eye opening at 64 Gbaud PAM4 while retaining strict linearity required for PAM4 amplitude integrity. A fully differential variable-gain amplifier (VGA) follows the CTLE and provides 9 dB programmable gain range to accommodate channel loss and optimize eye-level spacing. The VGA is implemented using Gilbert-cell based topology, ensuring gain control with minimal impact on bandwidth or linearity. A final $50\ \Omega$ differential output driver is provided to interface the receiver with high-speed test instrument. It delivers a differential output swing of 350 mVpp while maintaining proper impedance matching and minimal group delay distortion across the target frequency band. The total power consumption of the receiver front-end is measured as 84 mW under a 1.0 V supply, corresponding to an energy efficiency of 0.66 pJ/bit at 64 Gbaud PAM4.

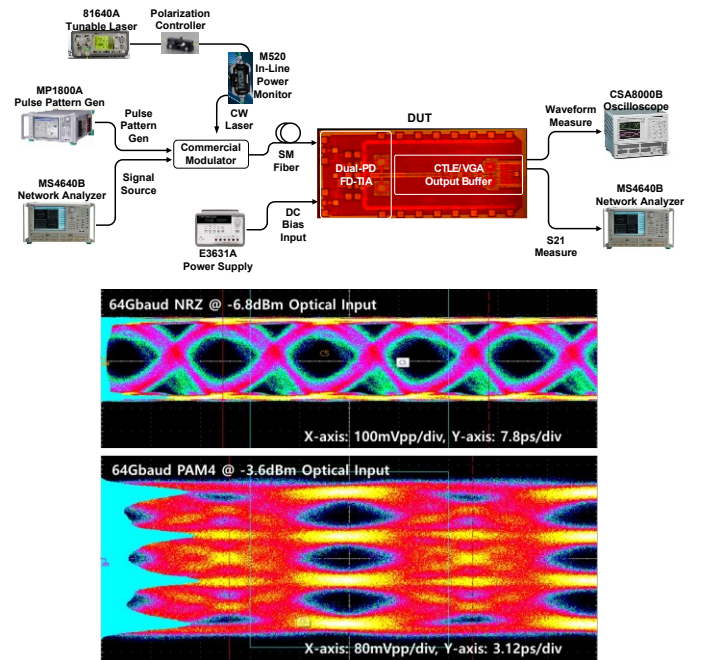


Figure 3. Measurement setup and measured eye patterns for 64Gbaud NRZ and PAM4.

IV. MEASUREMENT RESULTS

The proposed receiver was characterized using a commercial O-band optical modulator and a 64 Gbaud PAM4 pattern generator in a probe-based test environment. The small-signal transfer function was measured using a vector

network analyzer. The receiver exhibits a -3 dB bandwidth of 34.8 GHz, with < 2 dB gain peaking and a well controlled group delay across the operational spectrum. A PAM4 optical input through the commercial modulator with -3.6 dBm of optical power was applied at 64 Gbaud NRZ and PAM4, and the resulting electrical eye diagram was captured using a high-speed sampling oscilloscope. The measured PAM4 eye shows well-separated three-level amplitude spacing with 0.97 RLM, validating the linearity of the CTLE-VGA chain. The RMS output jitter was measured at 4.2 ps, and 0.36-UI horizontal eye opening was achieved.

V. CONCLUSION

A 64 Gbaud PAM4 fully-differential optical receiver front-end integrated with monolithic dual photodiode has been presented and experimentally verified. By directly generating differential photocurrents using a 1:2 MMI and dual photodiodes, the proposed architecture eliminates the fundamental bandwidth and common-mode rejection limitations of single-PD pseudo differential receivers. The receiver employs a fully-differential TIA followed by a CTLE-VGA linear amplification chain, enabling wideband PAM4 signal processing. Measurement results confirm 34.8 GHz bandwidth and 0.66 pJ/bit energy efficiency, validating the architectural advantages of fully-differential electronic-photonic optical receiver. These results demonstrate the suitability of the proposed receiver for next-generation AI datacenter and co packaged optical systems demanding high bandwidth density and low power consumption.

ACKNOWLEDGMENT

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