

DVB-S2 LDPC Finite-Precision Decoder

Sherif Welsen Shaker

Communications and Signal Processing Research Lab,
Faculty of Engineering, Ain-Shams University, Cairo, Egypt.

welsen@ieee.org

Abstract— The latest standard of Digital Video Broadcasting (DVB-S2) features a powerful forward error correction system. This is enabled by replacing the concatenated Reed-Solomon/convolutional coding approach of DVB-S with a concatenation of an outer BCH code and inner low-density parity-check (LDPC) code, which is considered one of the most powerful codes known today and it can even outperform Turbo-Codes. In the decoding of LDPC code, huge data processing, storage, and interconnect requirements is a real challenge for decoder realization. For decoder hardware implementation, reduced complexity leads to low power consumption which might be a key implementation issue. This paper investigates the effect of the number of iteration and the decoder's input quantization to achieve a significant improvement in the hardware implementation of the decoder architecture and hence leading to lower delay, higher throughput, reduction of area and power consumption in the whole radio receiver.

Keywords— Decoder Quantization, DVB-S2, Finite Precision, LDPC, Low-power, Reduced Complexity

I. INTRODUCTION

Digital Video Broadcasting (DVB) project was founded in 1993 by the European Telecommunications Standards Institute (ETSI) with the goal of standardizing digital television services. Its initial standard for satellite delivery of digital television, named DVB-S, used a concatenation of an outer (204,188) byte shortened Reed Solomon code and an inner constraint length 7, variable rate (r ranges from $1/2$ to $7/8$) convolutional code [1]. The same infrastructure used to deliver television via satellite can also be used to deliver Internet and data services to the subscriber. Internet over DVB-S is a natural competitor against cable modem and DSL technology, and its universal coverage allows even the most remote areas to be served. Because DVB-S only provides a downlink, an uplink is also needed to enable interactive applications such as web browsing. The uplink and downlink need not be symmetric, since many Internet services require a faster downlink.

One alternative for the uplink is to use a telephone modem, but this does not allow for always-on service, has modest data rates, and can be costly in remote areas. A more attractive alternative is for the subscriber equipment to transmit an uplink signal back to the satellite over the same antenna used for receiving the downlink signal. However, given the small antenna aperture and requirement for a low-cost, low-power amplifier, there is very little margin on the uplink. Therefore, strong FEC coding is desired. For this reason, the DVB

Project has adopted turbo codes for the satellite return channel in its DVB-RCS (Return Channel via Satellite) standard [2]. At the same time that the DVB project was developing turbo coding technology for the return channel, it was updating the downlink with modern coding technology. The latest standard, called DVB-S2 which is intended to provide Direct-To-Home (DTH) services for consumer Integrated Receiver Decoder (IRD), as well as collective antenna systems (Satellite Master Antenna Television - SMATV) and cable television head-end stations. DVB-S2 may be considered a successor to the current DVB-S standard. DVB-S2 is intended to provide interactive services to consumer IRDs and to personal computers. The return path can be implemented using various DVB interactive systems, such as DVB-RCS [3]. The new DVB-S2 standard features a powerful forward error correction system. This is enabled by replacing the concatenated Reed-Solomon/convolutional coding approach of DVB-S with a concatenation of an outer BCH code and inner low-density parity-check (LDPC) code [4]. LDPC code is considered one of the most powerful codes known today which can even outperform Turbo-Codes [5]. To provide flexibility, DVB-S2 specifies different code rates with a codeword length up to 64800 bits. The huge maximum codeword length is the reason for the outstanding communication performance ~ 0.7 dB to Shannon results and an increase of a 30% increase in capacity over DVB-S. The decoding of LDPC is an iterative process. At each iteration, a lot of data are scrambled and calculated. This huge data processing, storage and interconnect requirements is a real challenge for decoder realization, hence the outstanding coding performance of those codes requires the investigation of the hardware implementation issues. For portable radio, low power consumption is a key implementation issue. In this paper, application knowledge is exploited to significantly simplify high-level design towards lower implementation complexity by investigating the number of bits representing each message value and the maximum number of iterations used by the decoding algorithm.

II. DVB-S2 LDPC CODE

LDPC codes, first introduced by Gallager [6], have recently received a lot of attention because of their excellent performance on binary symmetric channel (BSC) as well as Additive White Gaussian Noise (AWGN) channel. Regular LDPC codes are specified by a very sparse parity check matrix with a small fixed number of 1's along all rows and with a small fixed number of 1's along all columns have good performance, but a little worse than turbo codes. However,

storage requirements are real challenge for decoder hardware realization. The most efficient implementation is always the tradeoff between hardware complexity and decoding ability and the process of deciding the accuracy of the finite precision representation and, hence, setting the parameters of fixed-point simulation, is also a tradeoff process. Instead of selecting these parameters in a late stage of the hardware simulation, they can be selected earlier in the stage of software simulation using fixed-point approach.

A. Decoder Quantization

All LDPC decoding algorithms are usually specified in the floating-point domain. To get an efficient implementation, fixed-point number representation has to be used, which implies transformation from floating-point to fixed-point. The primary goal of this quantization for hardware implementation is to find a fixed-point model that has all bits-widths as small as possible under the condition of an acceptable degradation of the coding performance. In hardware implementation, the reduction of data-path bit-widths, control complexity and memory size leads to a reduction of area and power consumption and an increase of speed. The input data quantization as well as the inner data quantization have major influence on the control complexity and directly determine the bit-width of data-path and memory size. The smaller the bit-widths of quantization, the better the performance of the decoder in terms of speed, area and the power consumption. The quantization also has its effects on the decoding performance and thus, the optimized quantization is a key issue for the implementation complexity.

B. Reduced Complexity Decoding Algorithm

As with the probability-domain Viterbi and BCJR algorithms [9], the probability-domain MPA suffers because multiplications are involved (addition are less costly to implement) and many multiplications of probabilities are involved which could become numerically unstable. Thus, as with BCJR algorithms, a log-domain version of the MPA is to be preferred. It was shown also that other decoding algorithms like Min-Sum algorithm can provide similar performance to ideal implementation but with lower computational complexity [10].

The number of maximum iteration also should be investigated before the implementation phase to determine the sufficient number of iteration processes the implemented decoder will perform. It's obvious that as the number of iterations increases, the Bit Error Rate (BER) would improve but at the expense of the frame's processing time or the delay and on the decoder complexity and hence the power consumption as well. It should be noted that the DVB-S2 standard is uncommitted with low latency requirements, so it employs strong coding over codewords of normal or short frame lengths, but although the standard was designed for low complexity in hardware, the length of the codewords makes this the most computationally intensive of LDPC codes described in current standards. It should also be noted that increasing the number of maximum iterations by a factor of 2

dose not necessarily double the total delay because not all frames will need to take that maximum number of iteration.

IV. SIMULATION AND RESULTS

A Matlab code is first driven to evaluate the performance of the DVB-S2 LDPC coding. **Figure 1** shows the influence of the code rate on the Frame Error Rate (FER) performance of the normal frame size of 64,800 bits while **Figure 2** shows the performance of short frame size of 16,200 bits. Unlike other DVB standards like DVB-RCS, DVB-S2 fixes the length of the encoder output not the value of the encoder input.

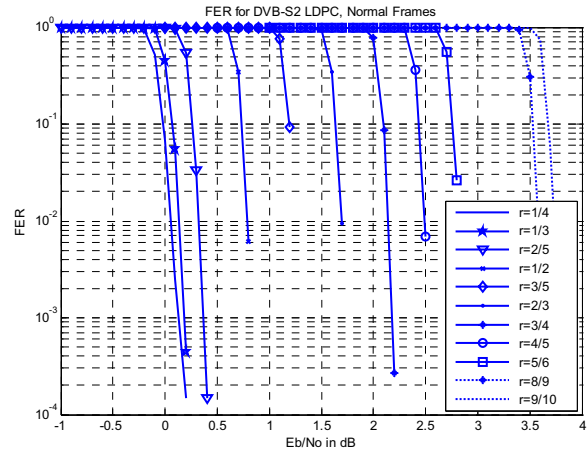


Figure 1. Influence of code rate on the FER performance of the normal frames DVB-S2 LDPC code.

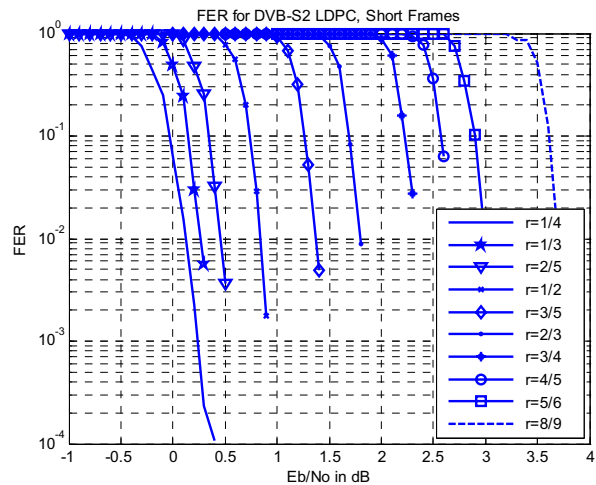


Figure 2. Influence of code rate on the FER performance of the short frames DVB-S2 LDPC code.

In our first simulation evaluating the performance of DVB-S2 standard, up to 100 iterations of the reduced complexity Minimum-Sum decoding algorithm were used. As stated before that only 10 out of 11 code rates are possible with the short frames, that the rate 9/10 is only available for long frames. For short frames, the rates 1/4, 1/2, 3/4, 4/5 and 5/6 are misnomers because the actual rates are 1/5, 4/9, 11/15, 7/9 and 37/45.

In order to simulate the real hardware, the investigation of the DVB-S2 LDPC performance has been made when numbers are represented in fixed-point format, instead of floating point one.

The investigation gives an insight into possible tradeoffs that can be done to achieve certain hardware complexity requirements. The effect of fixed-point implementation on the performance is measured by varying the number of bits representing each LLR value and the maximum number of iteration in the decoding algorithm. In **Figure 3**, a DVB-S2 LDPC short frame of rate 1/4 is used to study the effect of varying the number of iterations. It can be noticed a significant improvement when changing the maximum number of iterations from 10 to 100 iterations. It's obvious that 10 iterations are insufficient to get any acceptable performance but it's clear that as increasing the number of iteration, the performance improves. When going from 30 to 60 iterations the performance improves by 0.9 dB at FER = 2×10^{-2} . As increasing the number of iterations from 60 to 100 iterations, the performance improves by about 0.1 dB. This means that a little improvement will be gained for increasing the number of iteration further. From hardware implementation point of view, decreasing the maximum number of iterations will result in less more throughput and decoding delay.

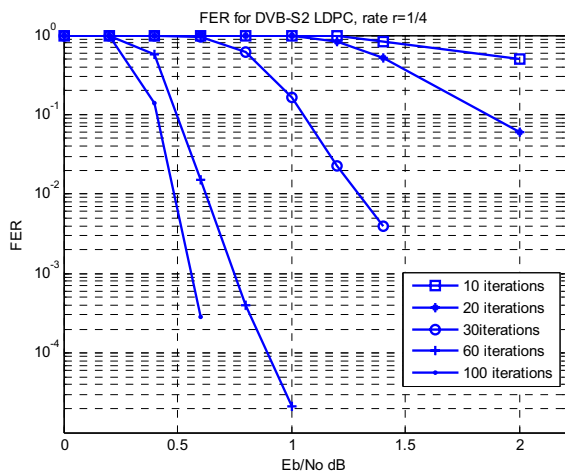


Figure 3. Influence maximum number of iterations on the FER performance of the DVB-S-2 LDPC code.

The number of bits used to represent LLR values is very important in the hardware implementation of an LDPC decoder. It will affect both of the speed, the performance, and the complexity. **Figure 4**, shows the simulation results of the DVB-S2 LDPC code for different bit resolutions. The simulation has been made on the short frame of rate 1/4 with a maximum number of iteration of 30 and the dynamic range is set to 7 while two different bit precisions 4-bit and 6-bit have been used. As it can be seen from **Figure 4** that the performance always improves with increasing the number of resolution bits and it can be shown that the decoder performance degradation when using 6-bit precision could be maintained at 0.1 dB compared with the floating point decoder.

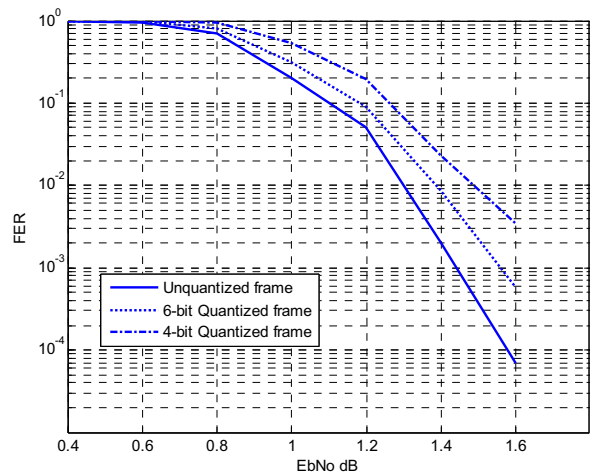


Figure 4. Influence of code rate on the BER performance of the DVB-RCS turbo code.

V. CONCLUSION

In this paper, an efficient decoder quantization for DVB-S2 LDPC coding has been made that reduces the complexity while realization of DVB-S2 radios. Performance simulation for varying of different supported code rates for such codes has been presented when changing the maximum number of iterations and results show that from 30 to 60 iterations could be used. Decoder quantization has been investigated and results show that 6-bits decoder quantization can be used with 0.1 dB degradation in performance than unquantized decoder

REFERENCES

- [1] European Telecommunications Standards Institute. "Digital broadcasting system for television, sound, and data services." *ETS 200 421*, 1994.
- [2] European Telecommunications Standards Institute. "Digital video broadcasting (DVB); interaction channel for satellite distribution systems;" *ETSI EN 301, 790 V1.5.1 (2009-05)*, 2009.
- [3] Sherif Welsen Shaker, Salwa H. El Ramly, and Khaled A. Shehata. "Design and Implementation of Adaptive Low-Power Turbo Encoder for DVB-RCS Software Radio", *Telecommunication Forum 2009 'TELFOR09'2009*, Belgrade, Serbia.
- [4] European Telecommunications Standards Institute. "Digital video broadcasting (DVB); Second generation framing structure, channel coding and modulation systems for broadcasting, Interactive Services, News Gathering and other broadband satellite applications." *DRAFT EN 302 307 DVBS2-74r15*, (2009-08).
- [5] C. Berrou, "The Ten-Year-Old Turbo Codes are Entering into Service", *IEEE Communications Magazine*, 41:110-116, Aug. 2003.
- [6] R. G. Gallager, "Low-density parity-check codes", *IRE Transactions on Information Theory*, vol. IT-8, pp. 21-28, Jan. 1962.
- [7] M. Yang, W. E. Ryan, and Y. Li, "Design of efficiently encodable moderate-length high-rate irregular LDPC codes" *IEEE Trans. Commun.*, 52:564-571, Apr. 2004.
- [8] D. J. C. MacKay, "Good error correcting codes based on very sparse matrices", *IEEE Trans. Inform. Theory*, 45:399-431, Mar. 1999.
- [9] P. Robertson, P. Hoeher, and E. Villebrun. "Optimal and sub-optimal maximum a posteriori algorithms suitable for turbo decoding", *European Trans. On Telecommun.*, 8(2):119-125, Mar./Apr. 1997.
- [10] A.H. Banihashemi, J. Zhao and F. Zarkeshvari, "On implementation of min-sum algorithm and its modifications for decoding LDPC codes", *IEEE Trans. Comm.*, Nov. 2004.