An Analysis of DDR Channel Signal Integrity on a High-Performance Computing Mainboard

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Abstract—This paper focuses on the design of a mainboard of a computing node, a component of the server platform that can compute high-performance big data operations at high speed. In particular, it describes the results of a signal integrity analysis of the signal channels between the memory and the CPU on the PCB of the mainboard equipped with multiple DDR5 memories to rapidly process complex operations. Signal integrity verification is possible by checking whether the signal including high frequency is reflected on the PCB line, data loss, or affected by the signals of adjacent channels when transmitted. This paper discusses the preparation elements, analysis method, and analysis results required for DDR channel signal integrity analysis.

Keyword—signal integrity, insertion loss, DDR, eye diagram, computing node

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