FPGA-based MLP Hardware Accelerator for Real-Time Destination Prediction in Autonomous Vehicles

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***(Pt9)Abstract*— We propose FPGA-based MLP (Multi-Layer Perceptron) hardware accelerator designed for real-time destination prediction in autonomous vehicles. As personalized destination prediction services in autonomous vehicle systems become increasingly sophisticated, there is a growing need to perform efficient and low-latency AI inference directly within vehicles rather than relying on cloud servers. However, software-based neural network inference on embedded processors creates performance bottlenecks that fail to meet the real-time requirements of autonomous vehicles. The proposed system implements MLP model that takes seven features as input—including Device ID, Device Type, latitude, longitude, time information—and predicts six destination classes. Developed using Vitis HLS on the Zynq-7000 SoC platform, the FPGA hardware accelerator achieves an inference time of 0.0055ms through AXI Stream interface, demonstrating a 68.5× performance improvement compared to ARM-based software implementation (0.374ms).**

***(Pt9)Keyword*—** Destination prediction, FPGA hardware accelerator, MLP neural network, Autonomous vehicles, Zynq SoC

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