HPPC: High-Performance Packet Cache for WAN Nodes with DDR Optimization

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***Abstract*—High-speed wide-area networks (WANs) exhibit large bandwidth-delay products (BDPs), so even modest random packet loss can drive congestion-controlled reliable transports far below line rate, motivating hop-local loss recovery at in-path devices. Realizing such hop-by-hop recovery requires buffering a sliding window of recently transmitted packets, yet commodity NICs and switches expose only limited on-chip SRAM, and naive use of off-chip DRAM incurs pointer chasing, poor row-buffer locality, and high read amplification. HPPC is a DRAM-resident packet cache that stores all buffered packets in a single circular buffer and maintains a compact, two-level flow-aware index, turning cache operations into predominantly sequential DDR accesses while elastically sharing capacity across flows. Implemented on a 100 Gb/s FPGA-based network card with dual DDR4 channels, HPPC sustains line-rate throughput for 1500-byte packets (approximately 8.3 Mpps) and, under 1% packet loss across more than 1,000 concurrent flows, maintains at least 94% of line-rate goodput on the protected WAN segment without requiring changes to TCP/RDMA endpoints.**

***Keyword*—Wide-area networks, packet caching, reliable transport, DDR, buffer management.**

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